The SKA Central Signal Processor Project status and Italian contribution

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PRIN-SKA ESKAPE Arcetri, Nov 30, 2018



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- What is the CSP
- A bit of history
- SKA LOW-MID central beamformer structure
 - Italian contribution
- Pulsar timing
- Pulsar search: structure and contribution
- Local monitor and control: contribution
- Plans for the bridging phase







A bit of history

- 2011: SKA Organization
 - Non profit organization
- 2 Phase deployment: SKA1 (10%) & SKA2
 - Huge instrument: 1024 stations SKA-LOW, 256 antennas SKA-HIGH 64 antennas SKA-SURVEY
 - 256.000 spectral channels, 50 ms time res. → correlator increases data volume
 - Real time pulsar search (2000 beams) and timing (16 beams)

• 2013: Consortium starts

Each consortium an independent entity, self funded

- Mid 2014: Cost cap x 8-10 times, rebaselining
 - Deleted survey telescope. ASKAP is SKA1 survey instrument
 - 64k spectral channels, 0.2-0.6 s integration time
 - 512 stations for SKA-LOW, 196 dishes (incl. MeerKAT) for MID

• 2015: PDR

- Multiple solutions presented \rightarrow downselection.
- CBF-LOW goes to CSIRO \rightarrow redesigned. Italy exits CBF-LOW
- 2017: Cost reduction effort
 - "slice" architecture for CBF mid, 133 dishes
- Sep 2018: CDR



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CDR 24 September 2019

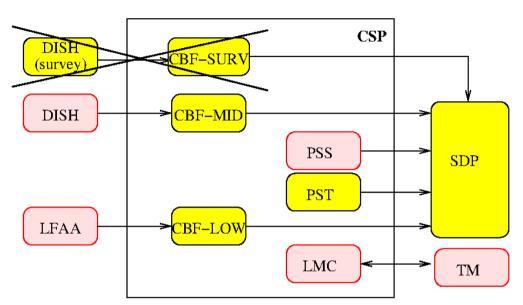


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SKA1-CSP STRUCTURE



Central Signal processor elements

- Central Beamformer: independent designs for Low and Mid
- Pulsar Search and Pulsar Timing machines
- Local monitor and Control

Concurrent Imaging, pulsar search, pulsar timing

INAF contributed elements / sub-elements in red

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SKA1-LOW Capabilities

Frequency range 50-350 MHz

- $Z = 4 \rightarrow 27$ for HI
- Pulsar timing at 200-350 MHz
- Velocity resolution:
 - $4 \rightarrow 30$ km/s (full BW), $0.2 \rightarrow 1.5$ km/s (zoom mode)
- Diameter = 38 m: FOV 1.5 10 deg
 - 256 antennas per station, up to 45 deg from zenith
- Maximum baseline 65 km: $2.8" \rightarrow 19"$ resolution
- 512 stations: 128K visibilities
 - Multiple sub-stations with reduced BW
- Sensitivity:
 - 550 m²-K between 100 and 350 MHz,
 - 60 m²-K at 50 MHz
- Multiple beams: up to 8 (less BW)
- Multiple sub-arrays (less stations)

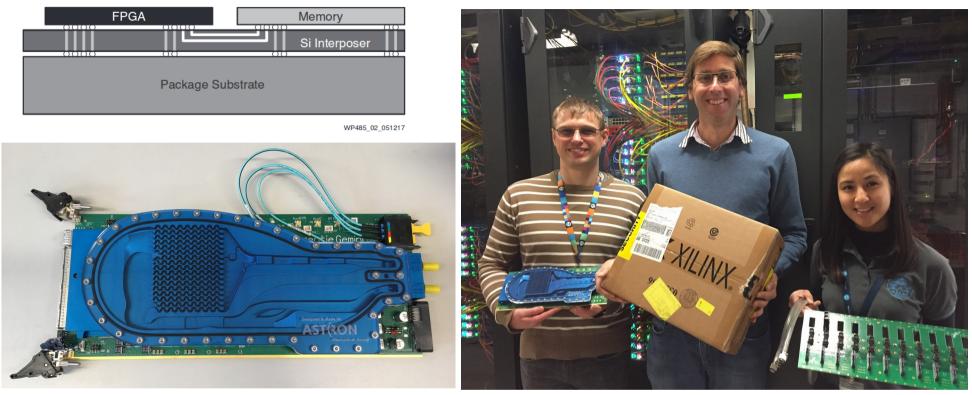
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CSP Low



- Architecture based on Xilinx High Memory Bandwidth FPGAs
- FPGA + memory chips in the same package
- Water cooled board in 3U subrack

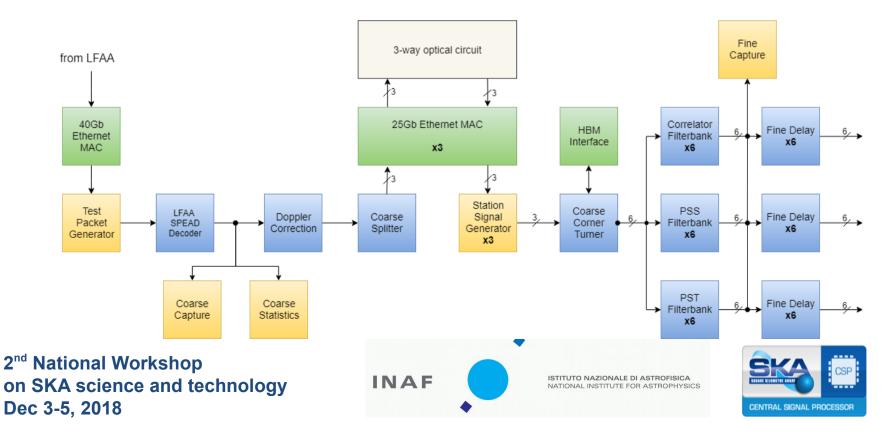
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FPGA processing

- Input data channelised by LFAA
- Channeliser for zoom mode resolution (226 Hz)
 - Other resolutions average channels in correlator very flat frequency response
- Doppler correction for system (telescope) and local (station) velocity



SKA1-MID Capabilities

- Frequency Range: 5 bands
- Frequency resolution:
 - Full band: BW/60,000
 - Zoom mode:
 - 250 Hz to 16 kHz resolution
 - 16,000 channels per window
 - 60,000 channels total
- Pulsar phase binning for time resolved pulsar images
 - Up to 1024 phase bins
 - Traded with spectral channels

| Band | Fmin (GHz) | Fmax (GHz) | BW (GHz) | # of slices |
|------|---------------|---------------|-------------|-------------|
| 1 | 0.35 | 1.05 | 0.7 | 4 |
| 2 | 0.95 | 1.76 | 0.81 | 5 |
| 3 | 1.65 | 3.05 | 1.4 | 7 |
| 4 | 2.80 | 5.18 | 2.38 | 12 |
| 5a | 4.70 | 8.50 | 3.9 | 20 |
| 5b | 8.30 | 15.30 | 2x2.5 | 26 |

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SKA1-MID Non imaging Capabilities

- Pulsar search: 1500 search beams inside main beam
 - One of the largest computing engine in the world, if built today
- Pulsar timing: 16 beams
- Transient buffer for FRB
- RFI detection flagging excision
- VLBI tied beam array

Limited concurrent operation of all capabilities



PSS prototype at Karoo

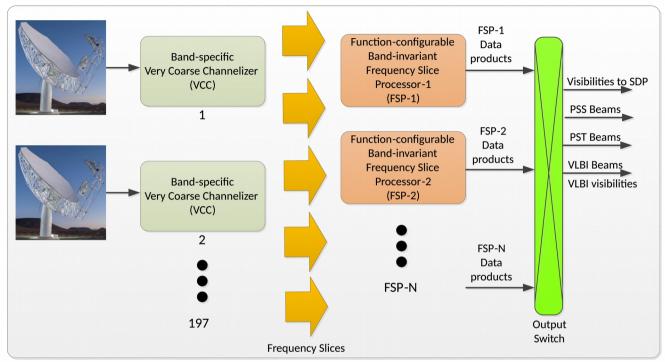
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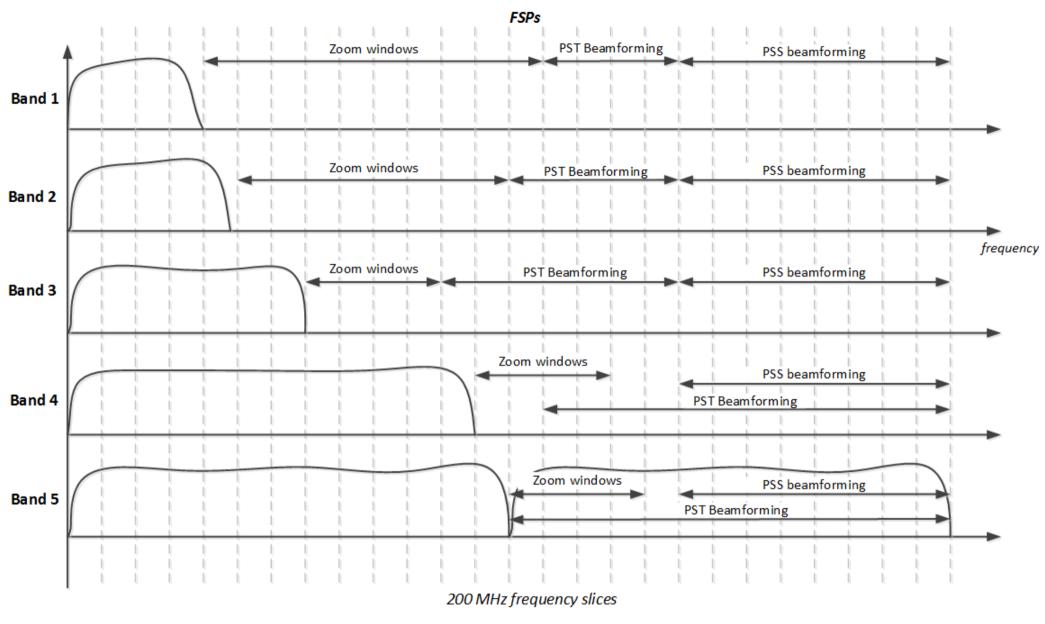
Slice structure for CSP-MID



- Correlator size determined by larger bandwidth (band 5)
- Divide input band into variable number of identical ~200 MHz slices
- Process each slice for imaging, zoom mode, PSS, PST or VLBI
- Full concurrent capability for lower bands
- Full band imaging mode for band 5, but not concurrent with PSS & PST

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"Commensality Diagram"

S7: CSP CDR Meeting: Sept 25-28, 2018



Italian contribution

- Design of key elements
 - Time domain delay
 - Correlator cell (complex multiplier)
- Modelling of fixed point effects
 - Finite step in delay/phase correction
 - Quantisation in digitiser
 - Quantisation in requantisaton stages
 - Harminic distortion due to requantisation

Two scientific publications (accepted)

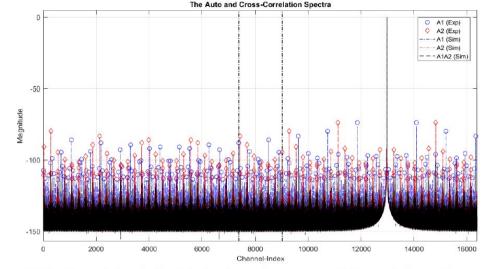
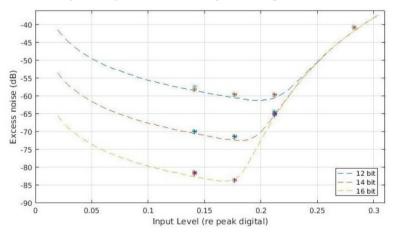


Figure 5-21 Expected and simulated auto- and cross- correlations of channelized ReSampler outputs with no delay dithering.



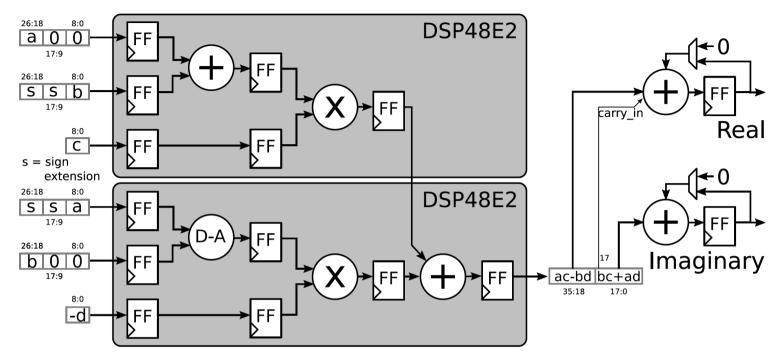
Added quantization noise for 12, 14, and 16-bit intermediate quantizations as a function of the input signal level.

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Matrix Correlator Cell



Basis of correlator

Both for Altera (MID) and Xilinx (LOW) architectures

Published in *Conference on Reconfigurable Computing and FPGAs (ReConFig 2018)*

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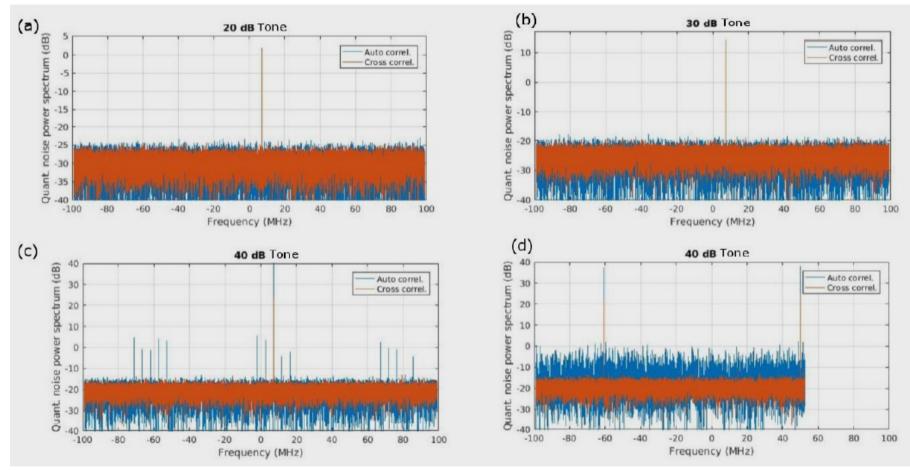
IMPLEMENTATION RESULTS FOR XILINX ULTRASCALE+

| Style | Width | LUTs | FFs | DSPs | Fmax |
|-----------|-------|------|-----|------|---------|
| optimised | 9-bit | 86 | 54 | 2 | 640 MHz |
| inferred | 9-bit | 99 | 163 | 2 | 450 MHz |





Modelling example



Quantisation noise for strong RFI – 8 bit ADC – SKA Mid band 1

RFI from 100 to 10⁴ times the broaddband sky signal

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Pulsar timing (PST)

- Prototype at MeerKAT.
 - 4 x Nvidia TitanX
 GPUs
 - Pulsar Timing & Dynamic Spectrum Modes
 - 2 x 856 MHz tiedarray beams
- Almost no Italian involvement
 - Some contribution to simulations



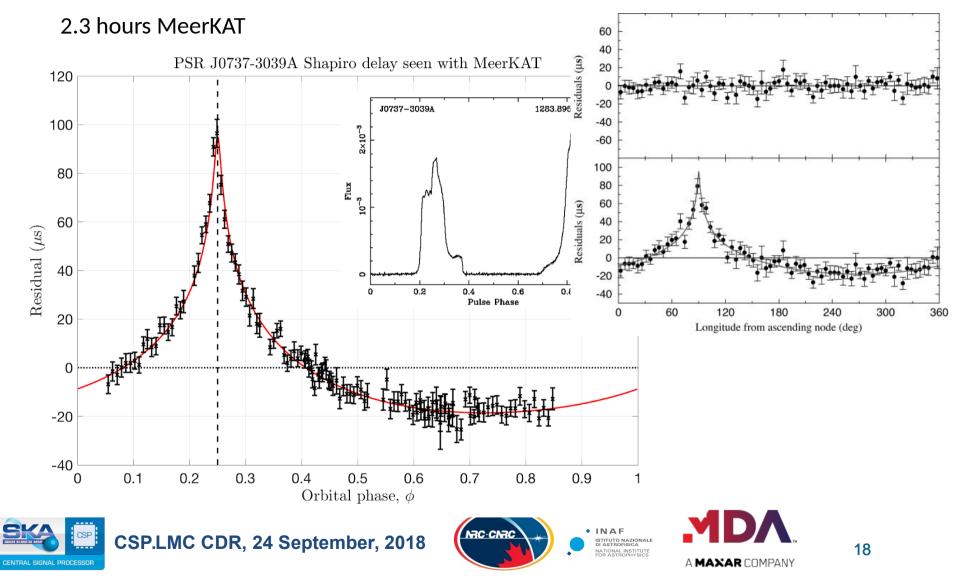
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Measurement of Shapiro Delay

7 months Lovell



Pulsar search (PSS)

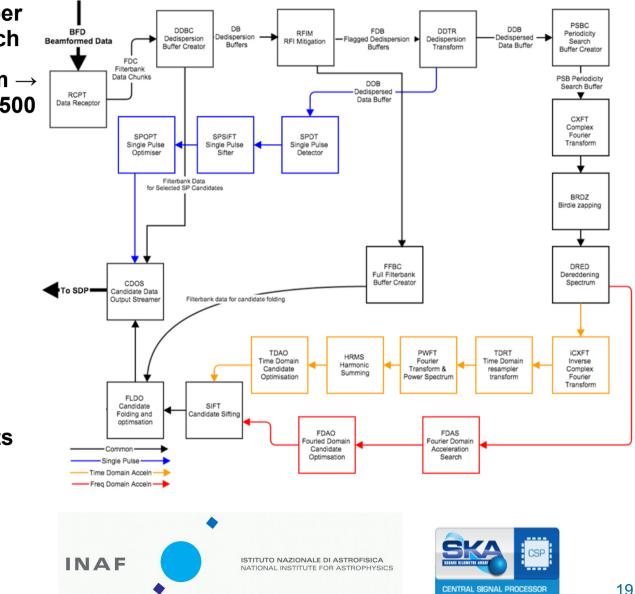
- Input data volume: 1 PB per pointing \rightarrow real time search
- Small interferometer beam \rightarrow large number of beams (1500 mid + 500 low)
- Unknown period and DM ٠
- Relativistic binaries \rightarrow • unknown acceleration **Dominant computational** request
- **Detection of FRB (for** ٠ detection capture)
- Power constraints

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Physical space constraints

on SKA science and technology



On site hardware prototype

ProtoNIP: a PSS prototype in the Karoo

- 18x 2U, dual socket, dual accelerator servers
- 2x Intel Xeon 14 cores
- Arria 10 PCIe FPGA board
- NVIDIA P100 GPU card
- 512 GB TruDDR4 RAM
- Rack allocation for tests of power, cooling, system stability, running Cheetah/Panda prototype software.
- Hardware all in place and operational.





CSP.LMC CDR, 24 September, 2018





PSS – Code Development

Red: Inaf contribution

- **GPU (DDTR/FDAS)**
- **GPU (FLDO)**
- LMC
- PANDA
- CHEETAH
- FPGA (DDTR/SPDT) --

- Signal Model

- -- 23,000 lines of code (Cuda/C++)
- -- 15,000 lines of code (Cuda/OpenCL)
- -- 10,000 lines of code (C++)
- -- 22,000 lines of code (C++)
- -- 31,000 lines of code (C++)
 - 1,500 lines of code (OpenCL)
- FPGA (CXFT/FDAS) -- 1,500 lines of code (OpenCL)
- FPGA (FDAS/FLDO) -- 40,000 lines of code (VHDL)
- CPU (TestVectors) -- 10,000 lines of code (python)
 - 12,000 lines of code (Matlab/C++)

UNIVERSITY OF

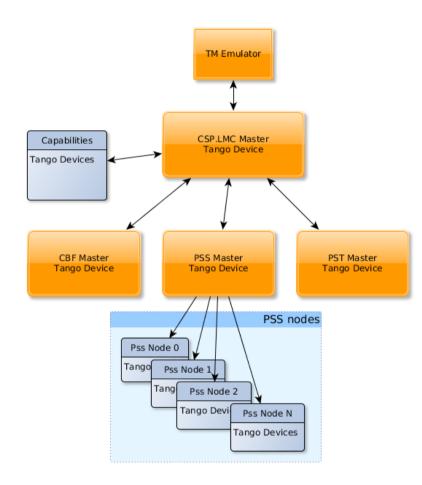
Part E: CSP CDR Meeting: Sept 25-28, 2018





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PSS Local Monitor & Control



90% Italian contribution

PSS LMC evolutionary prototype:

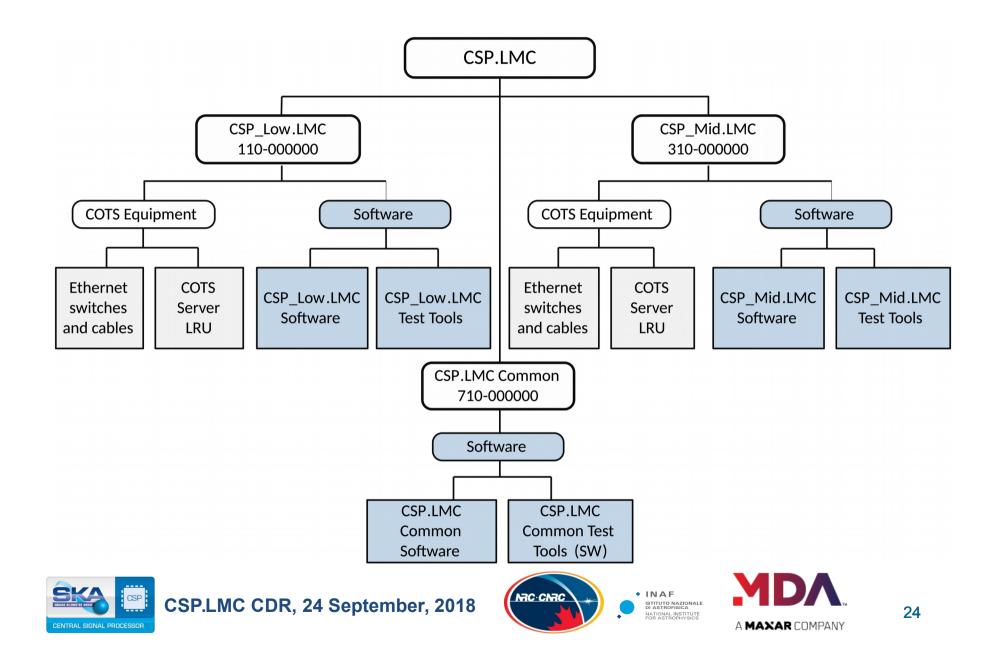
- Main Tango Control Devices in place.
- Init/program/start scan working. interface with (small) real nodes.
- Interface with simulated pipelines.
- Compatible with the (evolving) SKA standards.

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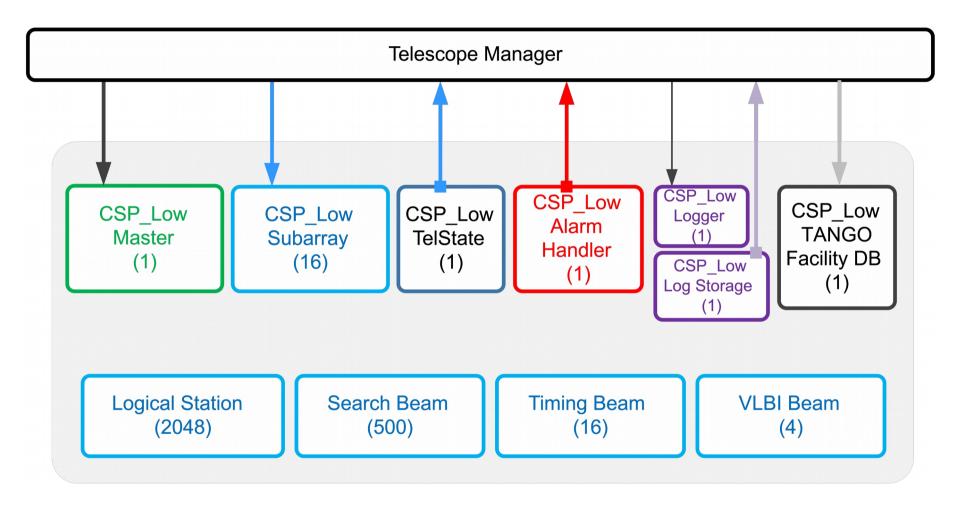




CSP Local Monitor and Control



CSP_Low - TM View (TANGO API)





CSP LMC prototyping









INAF contribution Summary & Bridging phase

• CBF

- Correlator cell structure
- Modelling quantization effects
- PSS
 - Folding-Optimization
 - Local Monitor & Control
- LMC
 - Prototype: test of the basic structure

Signal chain modelling

- Linearity
- RFI immunity

PSS prototype

 Increment of the Technological Readness Level: tests at MeerKAT

LMC Prototype

 Improve current prototype to a production level framework

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