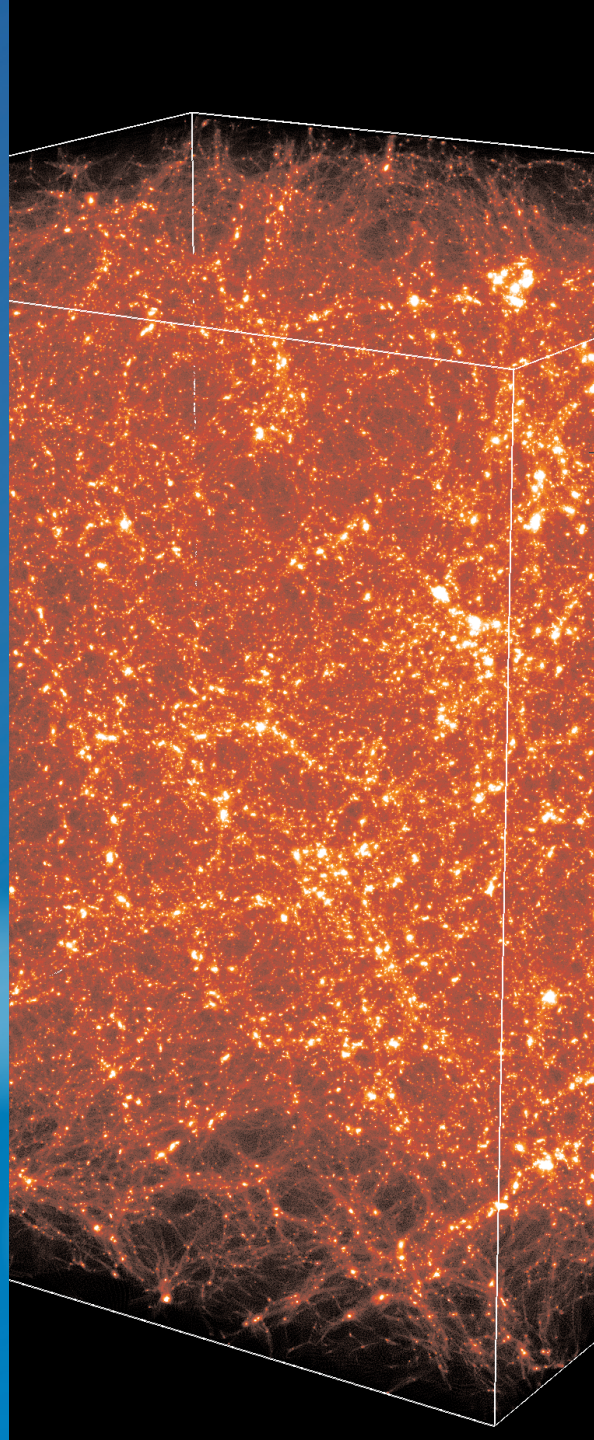
ITPM ADU 1.5 :

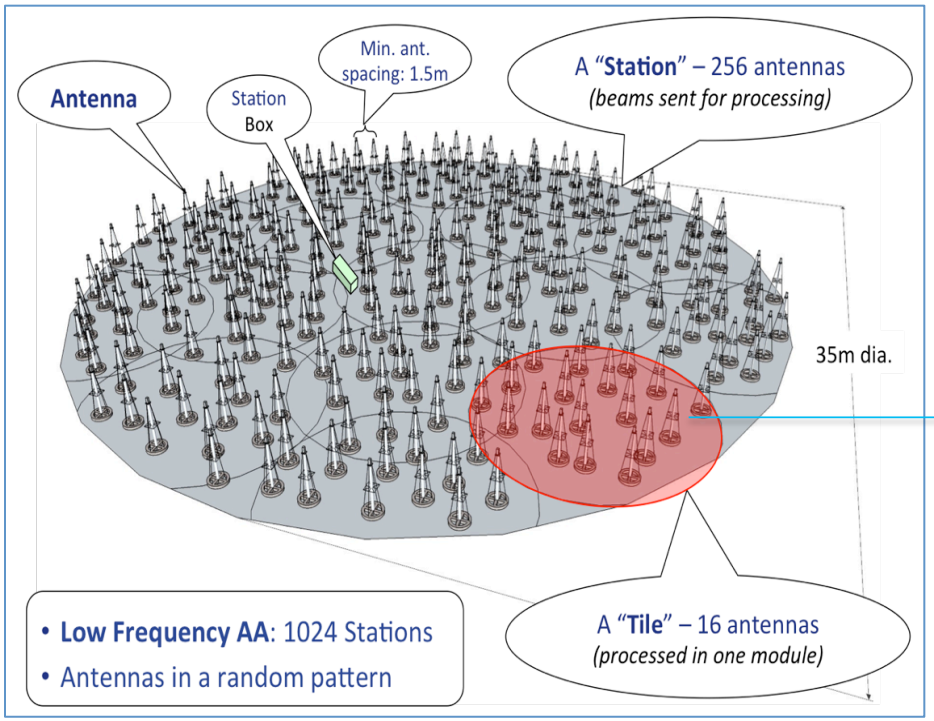
LFAA and ‘general purpose’ applications

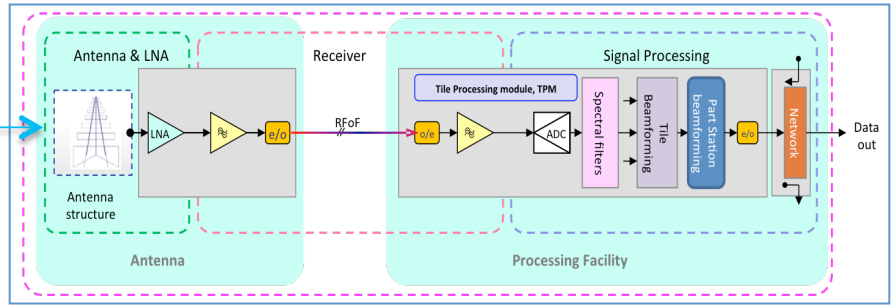


Francesco Schillirò
INAF-Osservatorio Astrofisico di Catania
Email : fschilliro@oact.inaf.it

Dec, 3 , 2018 – SKA ITALY

LFAA: Tile Processor Module





Tile: 16 Antennas, 2 Pol, 32 Channels.

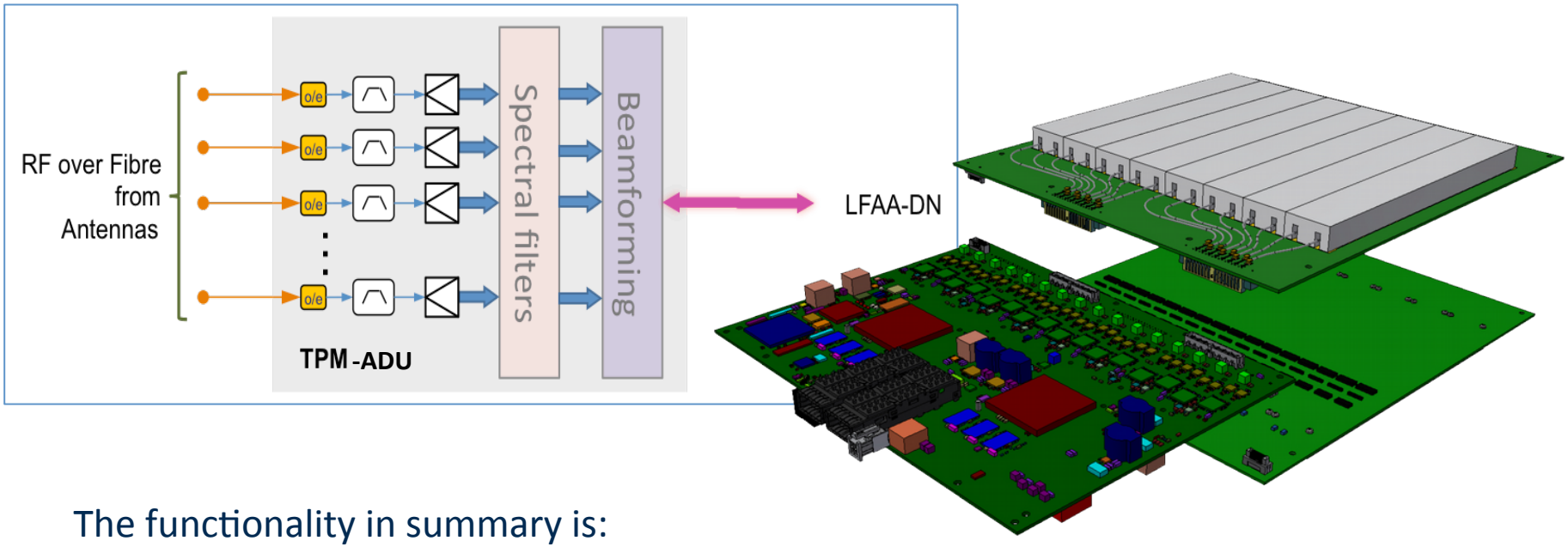
Exploring the Universe with the world's largest radio telescope

Tile Processor Module in AAVS1

Credit: ICRAR/Curtin University, Western Australia

Exploring the Universe with the world's largest radio telescope

ITPM functionality



The functionality in summary is:

- Convert analogue optical to electrical signals
- Amplify and bandpass filter ready for digitisation;
- Digitise at 800MS/s and pass to digital processing;
- Manage the clock distribution and the memory storage;
- Digitally process;
- Packetize Data for 100 Gbit/sec data processing;
- Control and monitoring processor data

ITPM-ADU Generations

ADU technical evolution

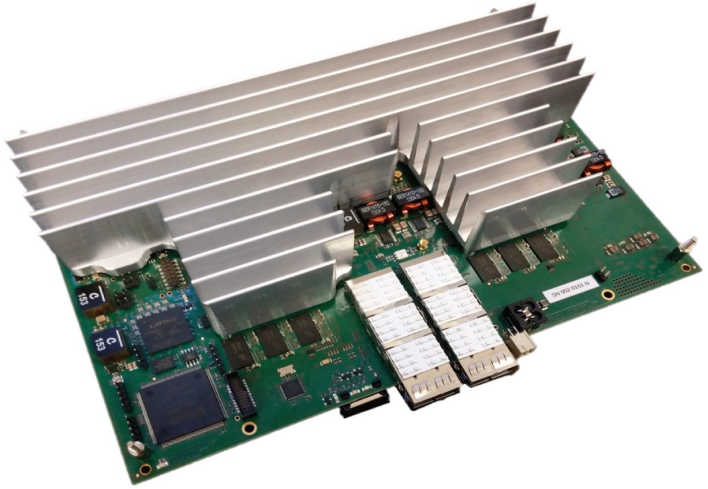
The ADU board has maintained the same component list and board architecture toward the successive release, only minor changes has been done:

- ADU 1.0 first release, main issue, input DC-DC supply under dimensioned and some component layout optimization needed for the soldering process (2013-2014)
- ADU 1.1 doubled the first DC-DC, corrected some minor bugs, 32 data channel acquisition and characterization done, product complete and stable (2015)
- ADU 1.2 the same BOM as 1.1 just some layout minor changes for ADC sampling clock equalization. ADU 1.1 and TPM-ADU 1.2 are firmware and software compatibles (2016)
- ADU 1.2 released and engineered as PAF digital processing solution (2017)
- ADU 1.5, released specification with the migration of the previous component list to the equivalent newer one, to reduce absorbed power 20% and cost. The board architecture, in terms of component placement, clock distribution and board structure will share the same specification of the ADU 1.0 to 1.2 (2018)
- ADU 1.6 as 1.5 minor upgrade (2019).
- ADU 2.0 with RFSoC design solution for PAF and Mid Frequency Array (2019).

ITPM ADU Versions 1.0 and 1.1

ITPM ADU 1.0 financed by Tecno INAF Funds:

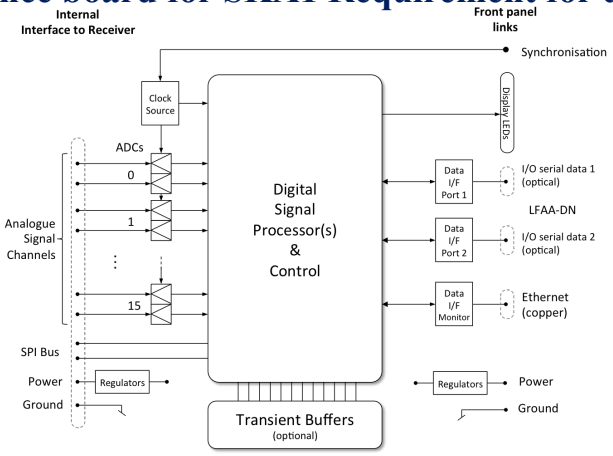
- **Designed Architecture**
- **Demonstrated feasibility and met most of the SKA Requirements**



ITPM ADU 1.1 Version
Has been designed in order to optimize

- **Power dissipation by introducing a new version of AD9680 ADC;**
- **Spurious Free Dynamic Range by mitigation of spurious frequencies distribution circuitry;**

ITPM ADU 1.1 final version for AAVS1 and SAD have been ordered by Oxford University and Cambridge University for SKA-MFAA prototypes .
ITPM 1.1 is the reference board for SKA1 Requirement for digital equipment.



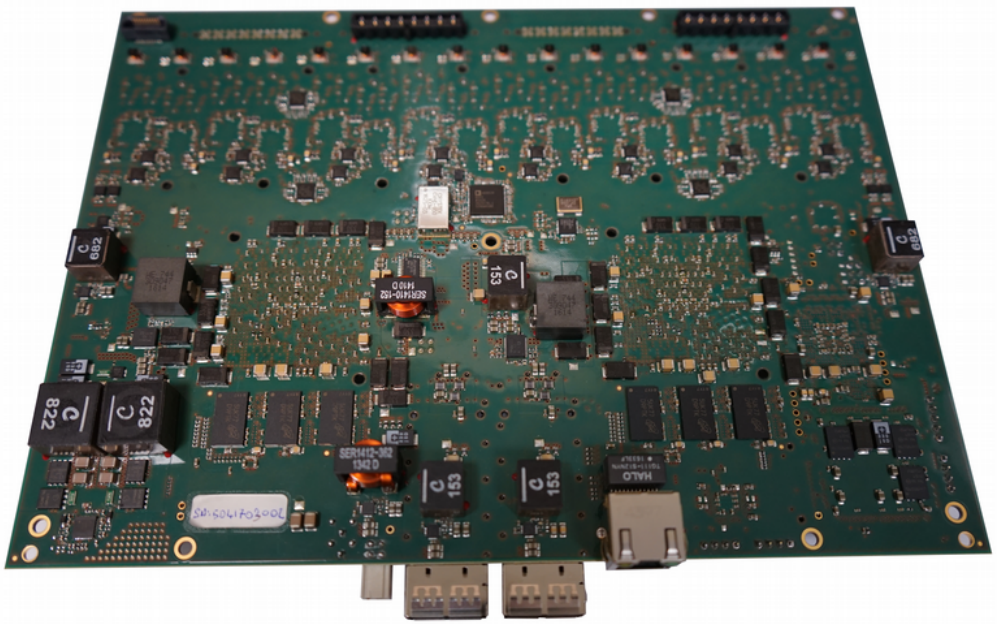
ITPM-ADU SPECS

Indicative Spec for SKA

Results for ITPM 1.0 (good candidates to be upgrated as 'Requirements'

SPEC Required	Fs: 800 MSPS --- BW: 50 – 375 MHz		
	ADC Perf. Parameters	ADU Board#1 (with ADA)	ADU Board#2 (without ADA)
>40dB	Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 49.19	≥ 49.33
+/- 1,5 dB	Gain Flatness [dBFS]	≤ ±0.3573	≤ ±0.343
	2nd-order Harmonic Distortion [dBc]	≤ -67.24 (3 points around 231.7 MHz)	≤ -67.74
	3rd-order Harmonic Distortion [dBc]	≤ -66.53 (3 points around 231.7 MHz)	≤ -68.56
<-40 dB	Worst Other Spur [dBc]	≤ -67.03	≤ -66.83
>40 dB	Spurious Free Dynamic Range [dBc]	≥ 66.53	≥ 66.83
> 6.5 bits	ENOB [bits]	≥ 7.876	≥ 7.896
-50 dB	Cross-Talk [dBc]	≤ -65.69	≤ -61
	IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	29.55	32.2
	IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	66.3	77.5
	Fs: 700 MSPS --- BW: 375 – 650 MHz		
	ADC Perf. Parameters	ADU Board#1 (with ADA)	ADU Board#2 (without ADA)
	Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 48.88*	≥ 49.32
	Gain Flatness [dBFS]	≤ ±0.6252	≤ ±1.356
	2nd-order Harmonic Distortion [dBc]	≤ -65.77*	≤ -59.9
	3rd-order Harmonic Distortion [dBc]	≤ -60.78*	≤ -65.64
	Worst Other Spur [dBc]	≤ -64.16*	≤ -63.23
	Spurious Free Dynamic Range [dBc]	≥ 60.78*	≥ 59.9
	ENOB [bits]	≥ 7.788*	≥ 7.886
	Cross-Talk [dBc]	≤ -70.58	≤ -70.39
	IP3 [dB] (F1=500.1 MHz; F2=503.2 MHz)	26	24.4
	IP2 [dB] (F1=500.1 MHz; F2=503.2 MHz)	64	58.3

ITPM-ADU Version 1.2: AAVS1



ITPM-ADU 1.2 final engineered version for AAVS1 and SAD

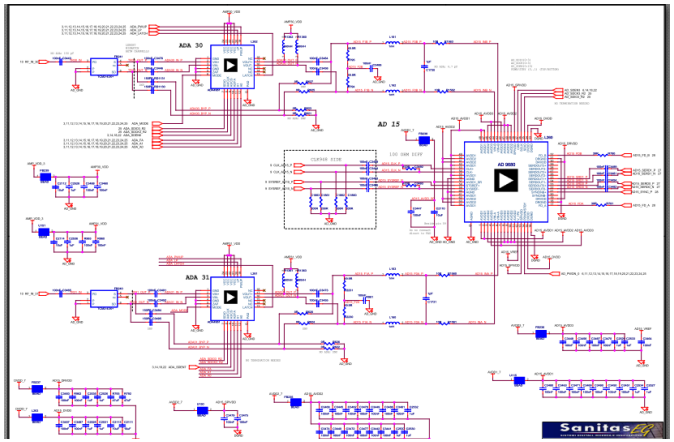
- 35 ADU Board produced (25 in Italy, 10 in The Nederlands);
- Designed lines engineered for mass production;
- Test benches produced both for prototypes as for mass production;
- Optimized design for Housing and Deployment

ITPM-ADU Version 1.2: AAVS1

Credit: ICRAR/Curtin University, Western Australia

- ITPM-ADU 1.2 connected to one "EDA" MWA station (16 Beamformed Tiles)
- ITPM-ADU 1.2 is one of the candidate FPGA-based board for use on ALPACA project (PAF at Arecibo Observatory)
- ITPM-ADU 1.2 CASPERized in august 2018 (now in progress, thanks to Naldi, Mattana et al.)

ITPM ADU Design: ADC



ANALOG DEVICES

14-Bit, 1300 MSPS/625 MSPS, JESD204B, Dual Analog-to-Digital Converter

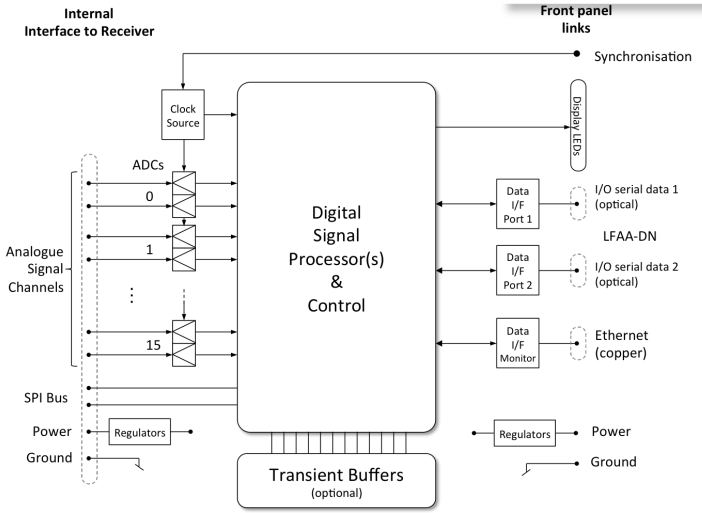
Data Sheet **AD9695**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 16 Gbps
- 1.6 W total power at 1300 MSPS
  - 800 mW per ADC channel
- SNR = 65.6 dBFS at 172 MHz (1.59 V p-p input range)
- SFDR = 78 dBFS at 172.3 MHz (1.59 V p-p input range)
- Noise density
  - −153.9 dBFS/Hz (1.59 V p-p input range)
  - −155.6 dBFS/Hz (2.04 V p-p input range)
- 0.95 V, 1.8 V, and 2.5 V supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible input range
  - 1.36 V p-p to 2.04 V p-p (1.59 V p-p typical)
- 2 GHz usable analog input full power bandwidth
- >95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- 2 integrated digital downconverters per ADC channel
  - 48-bit NCO
  - Programmable decimation rates
- Differential clock input
- SPI control
  - Integer clock divide by 2 and divide by 4
  - Flexible JESD204B lane configurations
- On-chip dithering to improve small signal linearity

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, WCDMA, GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation
  - Oscilloscopes
  - Spectrum analyzers
  - Network analyzers
  - Integrated RF test solutions
- Radars
- Electronic support measures, electronic counter measures, and electronic counter-counter measures
- High speed data acquisition systems
- DOCSIS 3.0 CMTS upstream receive paths
- Hybrid fiber coaxial digital reverse path receivers
- Wideband digital predistortion



Characteristic	Unit	Baseline Specification*	Minimum	Typical	Maximum
Sampling Bandwidth	MHz	300	300	400	500
ENOB	Bits	8	6	8	12
Power consumption	W	100	50	100	350
Channel isolation (for multi-channel ADCs)	dB	100	65	100	120
Max input RF power	dBm	-19	-40	-19	0
DSP Capability		No	NO	YES	YES
DNL	Bit	+/- 0.5 LSB	+/- 0.5 LSB	+/- 0.5 LSB	+/- 0.5 LSB
INL	Bit	+/- 1 LSB	+/- 1 LSB	+/- 1 LSB	+/- 1 LSB

TPM Devices: Xilinx Ultrascale

FEATURES OVERVIEW	
16nm low power FinFET+ process technology from TSMC Industry leading process from the #1 service foundry delivers a step function increase in performance-per-watt	▪ Over 2X performance-per-watt over Kintex-7 FPGAs ▪ The same scalable architecture and tools from Kintex UltraScale FPGAs
UltraRAM™ for deep memory buffering Up to 36Mb for SRAM device integration	▪ For deep packet and video buffering ▪ 8X capacity-per-block vs. traditional embedded memory ▪ Deep-sleep power modes
SmartConnect technology System-wide interconnect optimization tools and IP	▪ Matches optimal AXI interconnect to the design ▪ Automatic interface bridging ▪ Additional 20-30% advantage in performance-per-watt
Massive I/O bandwidth and dramatic latency reduction 50% greater serial bandwidth than Kintex UltraScale devices, and 4X greater than Kintex-7 devices	▪ 16G and 28G backplane support ▪ 32.75G chip-to-chip and chip-to-optics support ▪ High-Density I/O for greater area and power efficiency per pin
Next-generation routing, ASIC-like clocking, and enhanced fabric Enabling breakthrough speeds with high utilization	▪ Smaller area and greater power consistency ▪ Up to two speed-grade advantage vs. comparable solutions ▪ Efficient CLB use and placement for reduced interconnect delay
Massive memory interface bandwidth Next generation DDR and serial memory support	▪ DDR4 support of up to 2,666Mb/s ▪ Support for server-class DIMMs (8X capacity vs. Kintex-7) ▪ Hybrid Memory Cube serial memory support of up to 30G
PCI Express® integrated blocks Complete end-to-end solution for multi-100G ports	▪ Gen3 x16 and Gen4 x8 for 100G bandwidth per block ▪ Expanded virtualization for data center applications ▪ Enhanced tag management for increased buffer space
Integrated 100G Ethernet MAC and 150G Interlaken Cores ASIC-class cores for breakthrough performance in packet processing	▪ 60K-100K system logic cell savings per port ▪ Up to 90% dynamic power savings vs. soft implementation ▪ Built-in RS-FEC (Ethernet MAC) for optics error correction
Enhanced DSP slices for diverse applications Enabling a massive jump in fixed- and floating-point performance	▪ Up to 6.3 TeraMACs of bandwidth at 891 MHz operation ▪ Double-precision floating point using 30% fewer resources ▪ Complex fixed-point arithmetic in half the resources
High-speed memory cascading Removes key bottlenecks in DSP and packet processing	▪ Eliminates fabric usage when building deep memories ▪ Reduces routing congestion ▪ Lowers dynamic power consumption
Up to 50% power savings over Kintex-7 devices, and 30% power saving over Kintex UltraScale devices Static- and dynamic-power optimizations at every level	▪ Optimal voltage tuning ▪ Power-optimized transceivers and block RAM ▪ More granular clock gating of logic fabric and block RAM

XILINX
ALL PROGRAMMABLE™

Kintex Ultrascale 40 nm

Device Resources

	XCKU035	XCKU040	XCKU060	XCKU075	XCKU100	XCKU115
Logic Cells	355,474	424,200	580,440	756,000	985,440	1,160,880
Block RAM (Mb)	19.0	21.1	38.0	41.8	59.1	75.9
DSP Slices	1,700	1,920	2,760	2,592	4,200	5,520
PCI Express® Blocks	2	3	3	4	6	6
GTH 16 Gb/s Transceivers	16	20	32	52	64	64
I/O Pins	520	520	624	728	832	832
I/O Voltage	1.0V - 3.3V	1.0V - 3.3V	1.0V - 3.3V	1.0V - 3.3V	1.0V - 3.3V	1.0V - 3.3V

Kintex Ultrascale+ 16 nm

xploring the Universe with the world's largest radio telescope

Goal: reduce power consumption

Peripheral \ Board Release	R 1.2	R 1.5	R1.5 option
Digital IC			
CPLD, Eth, Flash, ...	3	2	
CPU	0,5	0	
FPGA, x2	55	52,0	40
DDR memories (*1)	3,4	5	
ANALOG (800 Mhz)			
PLL, CLKBuff, 10G PII	3,6	3,6	1,6
ADC	52,6	25,1	
VGA		7,128	
FRONT END	16,7	10,6	
Power distribution efficiency:			
Digital:	90,25%		
Analog (150 mV linear drop):	82,1%		
TOTAL DIGIT IC, Watt:	68,6	65,4	52,1
TOTAL ANALOG IC, Watt:	68,4	43,6	41,2
Front End	18,5	11,7	11,7
TOTAL Supply, Watt:	155,5	120,7	105,0

L'array di memoria cambia da DDR3L da 2 GB a DDR4 da 16 GB più grande, con la stessa velocità.

Part Number
XCKU9P-1FFVE900E
XCKU9P-L1FFVE900I
XCKU9P-L2FFVE900E

22% or 27% FPGA power consumption reduction

52% ADC power consumption reduction

GOAL: less than 70 W (only ADU)

Total power consumption reduction 22% or 32%

Power is estimated with maximum toggle rate , as simulating worse functional conditions

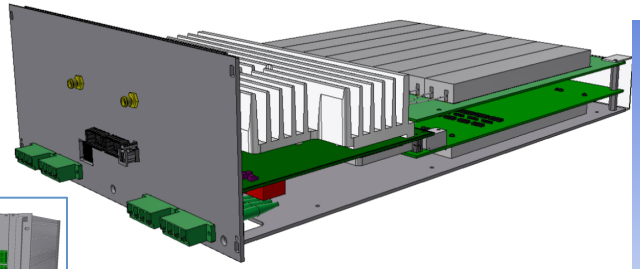
ITPM ADU Version 1.5

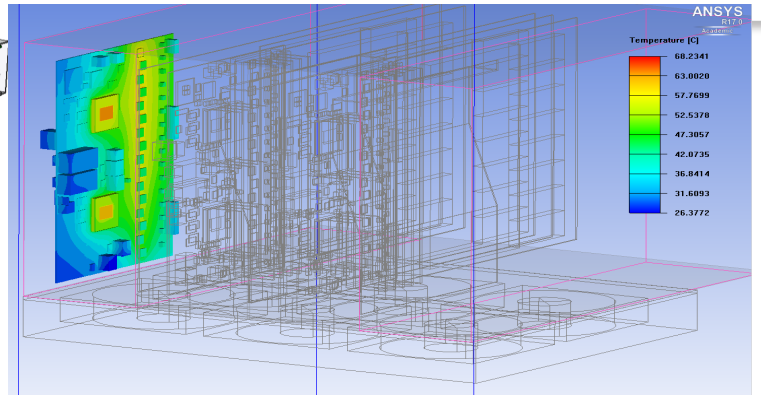
ITPM-ADU 1.5 is the reference design for LFAA Critical Design Review , and (one of) the candidates to be the digital platform for SKA1 –Low:

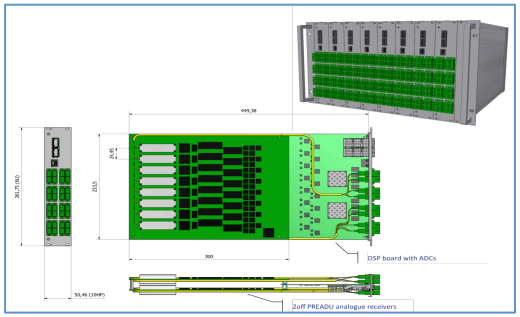
It's foreseen for this version:

- **New ADCs AD9695 low power Devices in order to minimize power dissipation;**
- **New DDR4 high-speed access and low power than DDR3 memories , 2Gbyte per FPGA;**
- **16 nm Kintex Ultrascale+ FPGA.**
- **100 Gb/sec digital data flow;**
- **Full Engineered ITPM Version for mass production**

LFAA Rack design and Electronics Housing







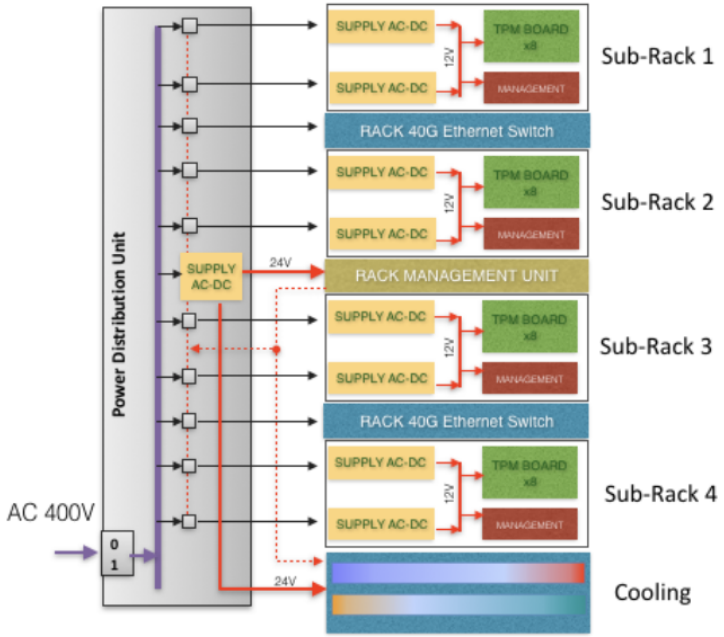
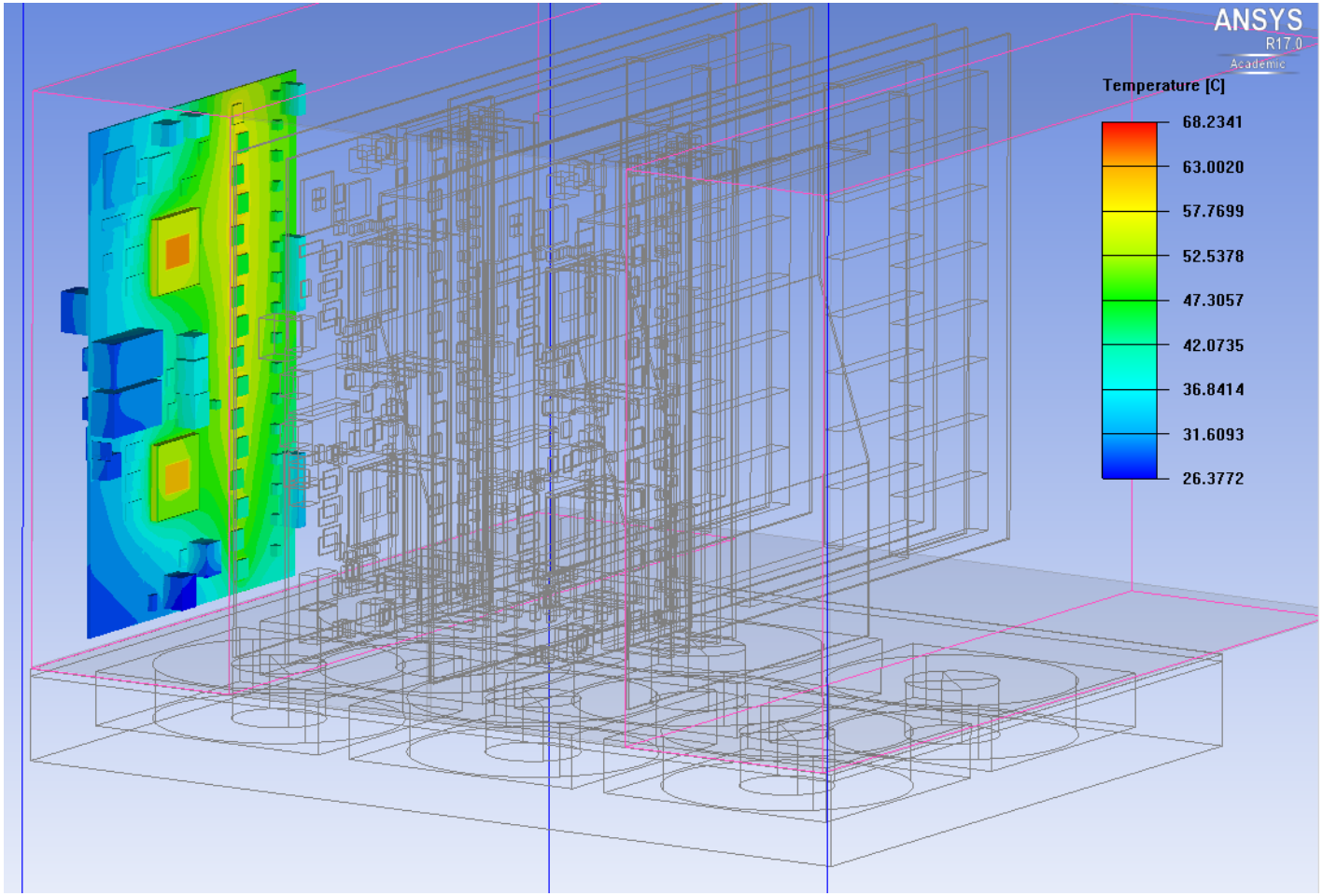


Figure 2 LFAA Cabinet power distribution scheme

telescope

RF Performances



SubRack Thermal Analysys

ITPM and SAD

Sardinia Array Demonstrator (SAD)

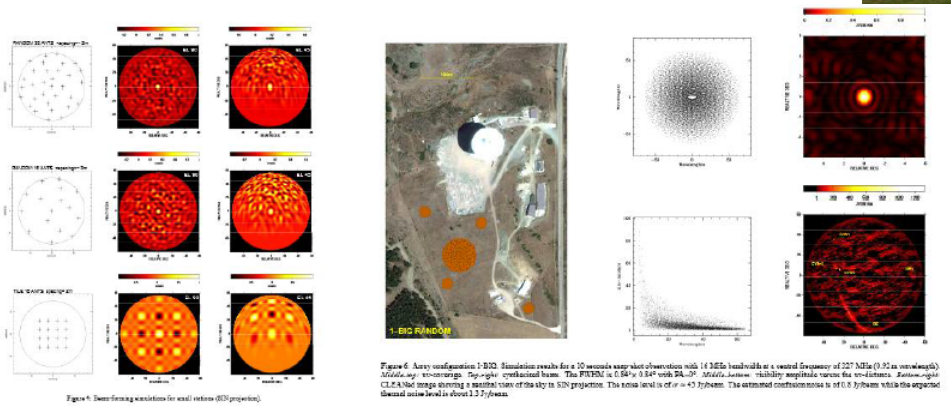


Fig 1. Preliminary study of array configuration, engineering and on site deployment

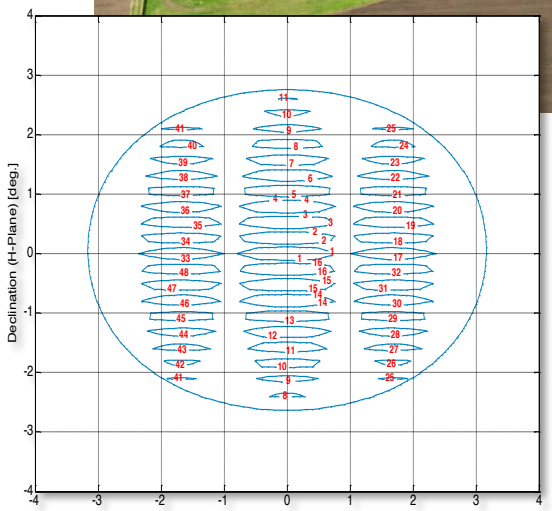
Exploring the Universe with the world's largest radio telescope

ITPM further Applications: SST

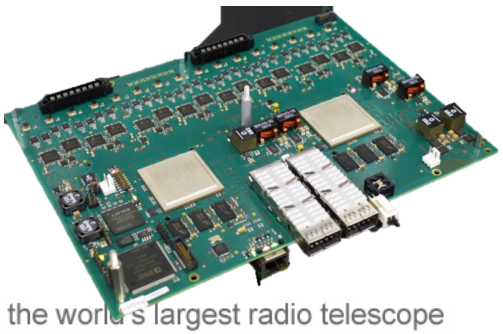
Medicina Northern Cross radiotelescope

Total collecting area = 28000 m²
N. of dipoles on the focal lines = 5632
Frequency = 16 MHz @ 408 MHz

Application in SST (Space Surveillance and Tracking) for the monitoring of orbiting objects

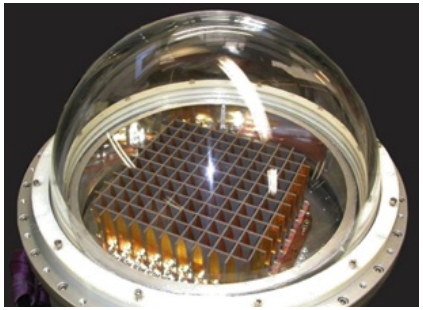


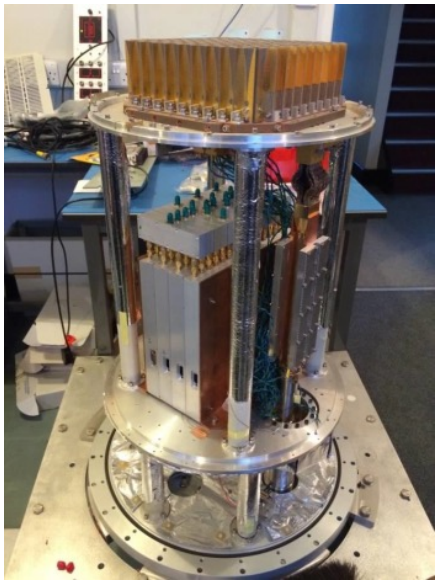
- Part of the Northern Cross radiotelescope has been refurbished within the SST program
- 64 new receivers have been installed
- A new multibeam on iTPM is under design/development



ITPM for PHAROS 2

- PHAROS2: C-band (4-8 GHz) cryogenically cooled low noise Phased Array Feed (PAF) demonstrator
- SKA Advanced Instrumentation Program on PAF
- To be installed in Lovell Radiotelescope (UK)



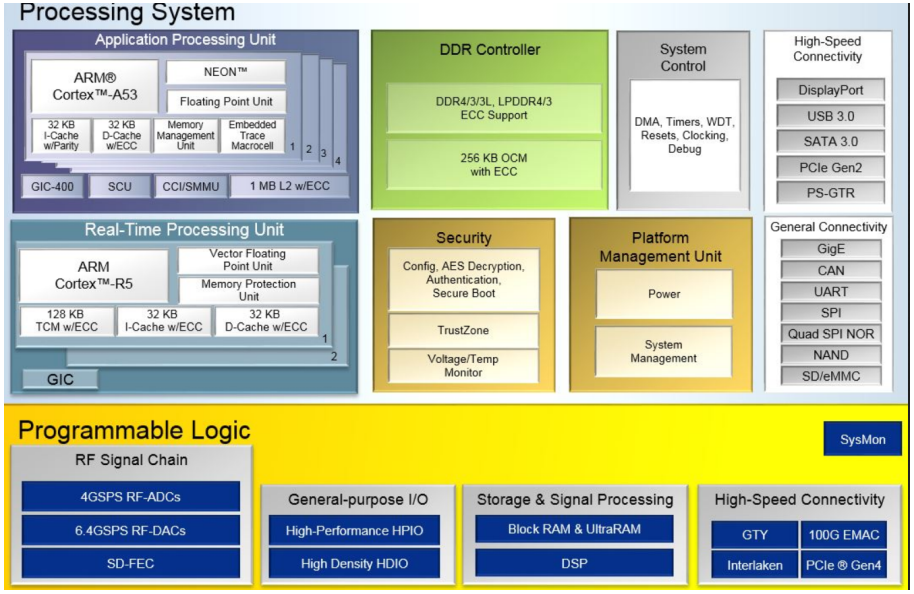


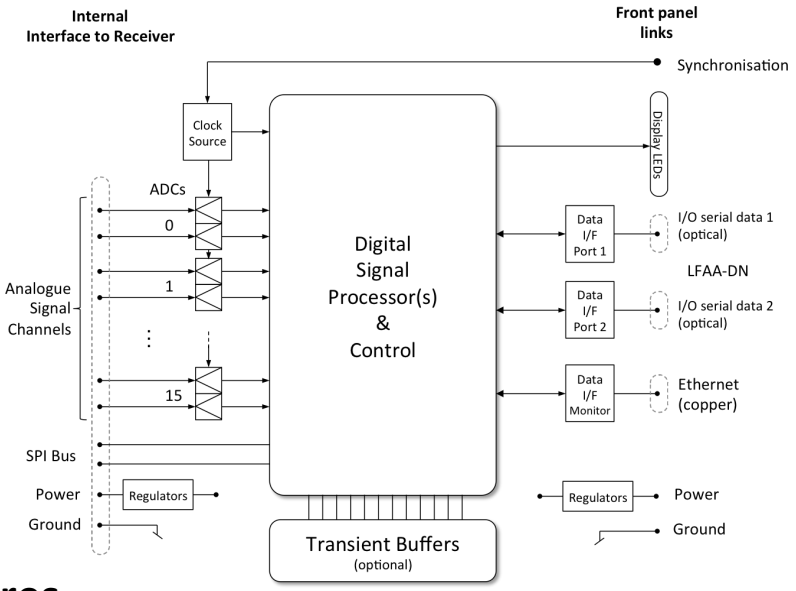
Digital Back end

- ADU board for digital acquisition and signal processing
- Frequency domain beamformer
- 4 independent single-pol. beams with ≈275 MHz bandwidth across 375-650 MHz
- 24 active elements of an array of Vivaldi antennas
- Same PFB architecture as in LFAA but
  - Different sampling rate: 700 MS/s
  - Simplified beamformer architecture
  - Include correlations with a calibration signal?

A. Navarrini et al. (2018), "Design of PHAROS2 Phased Array Feed", 2nd URSI AT-RASC, Gran Canaria

ITPM for PAF: RFSoC





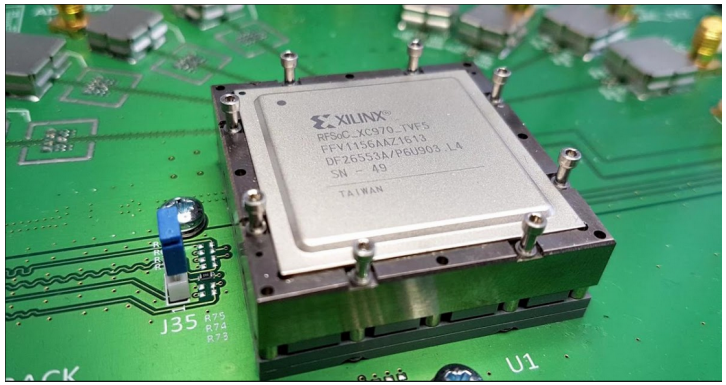
Featuring 8x8 RF-Analog and Integrated SD-FEC Cores

- **8x 4GSPS 12-bit ADCs**
- **8x 6.4GSPS 14-bit DACs**
- **Over 42 Gb/s LDPC FEC Encode System Throughput**
- **10Gb/s LDPC FEC Decode Throughput**
- **Support for custom LDPC Code Construction**
- **Over 7 Gb/s Turbo Decode System Throughput**

ITPM for PAF: RFSoC

Pros

1) The most important and sensitive functional blocks integrated
2) More robustness in design and functionalities
3) Less power consumption;
4) Smaller size and more subR integration



Cons

1) High costs (at the moment, it depends on Xilinx commercial strategy)
2) Feasibility study not ready yet (3D EM analysis, clock distribution, enob, etc.)
3) Performances not yet clear;
4) Power reduction not so relevant;
5) Effort (hr and funds) already invested in LFAA;
6) LFAA reference design robust and mature for mass production

CONCLUSION

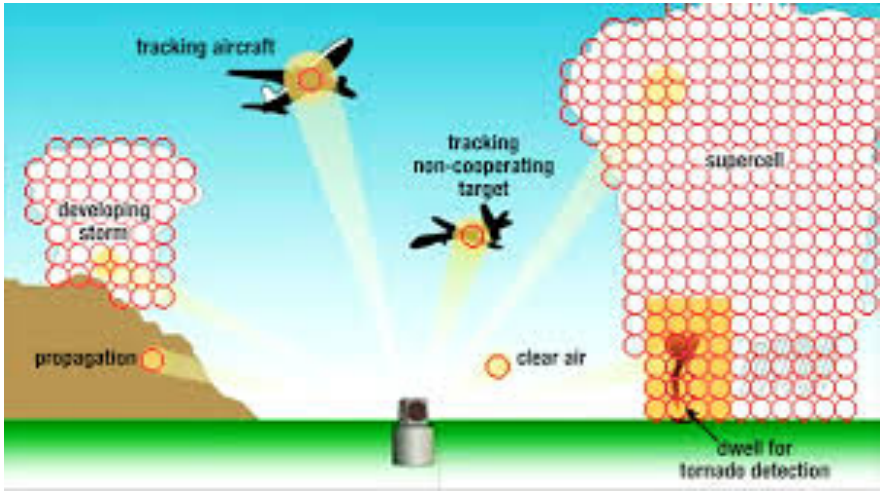
No sense to change technology NOW for LFAA

Strong interests to explore RFSoC for PAF…

fundraising machine is warming up….

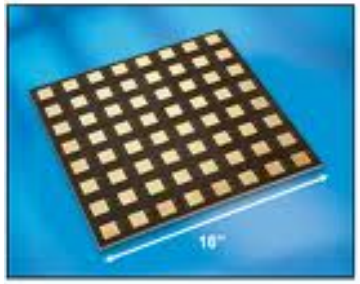
ITPM-ADU further Applications

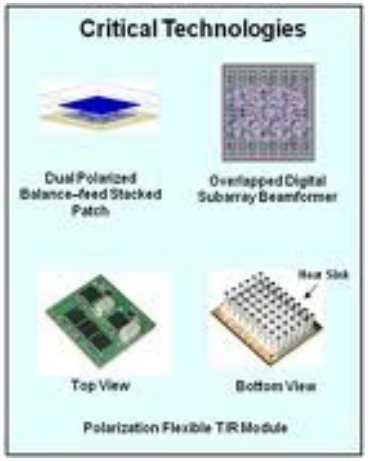
Aerospace



HPC Accelerator

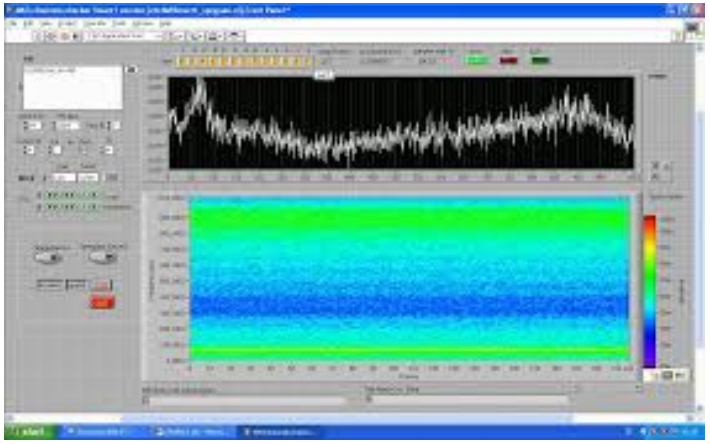
TLC





ITPM further Applications

Space Debris (Northern Cross)



ld's largest radio telescope

ITPM People

INAF

- Francesco Schillirò
- Gianni Comoretto
- Giovanni Naldi
- Andrea Mattana
- Monica Alderighi
- Jader Monari
- Federico Perini
- Giuseppe Pupillo
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- Sandro Pastore
- Fabio Casini

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- Amin Aminaei

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- Gabriele Dalle Mura
- Emanuele Zaccaro

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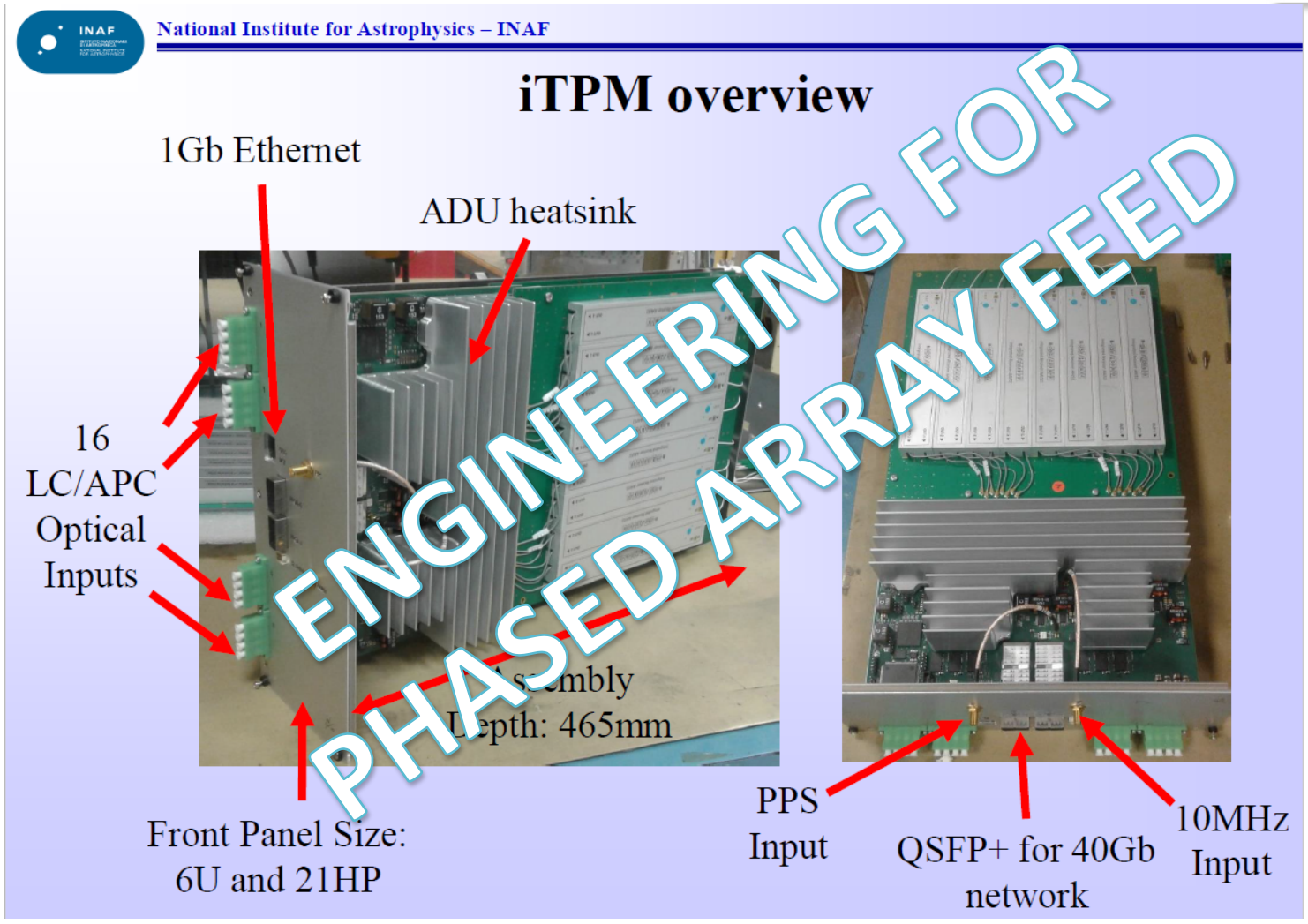

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