iTPM

italian Tile Processing Module

ICT Workshop 2017 – Bologna

Andrea Mattana

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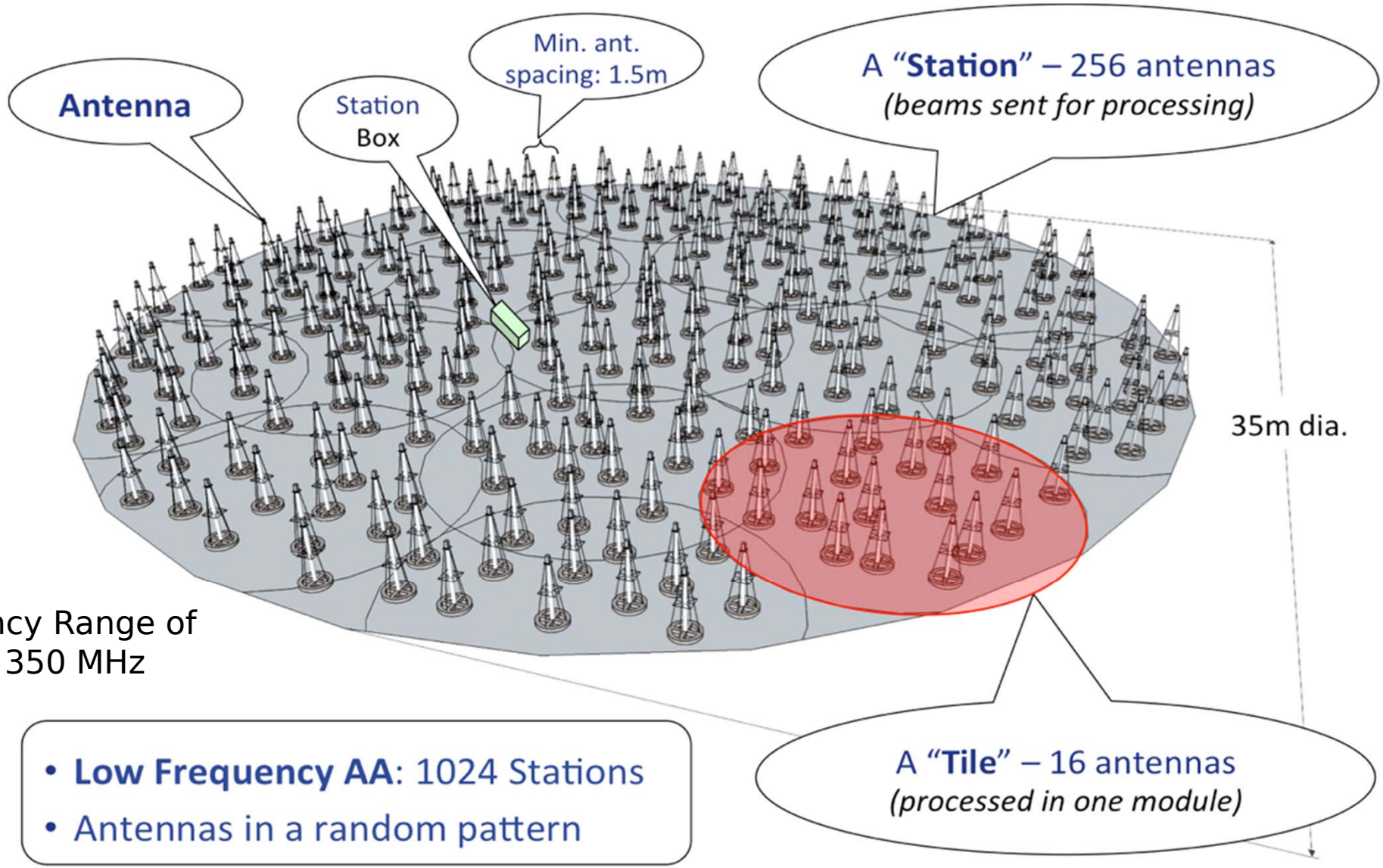

Frequency Range of
50 – 350 MHz

- **Low Frequency AA**: 1024 Stations
- Antennas in a random pattern

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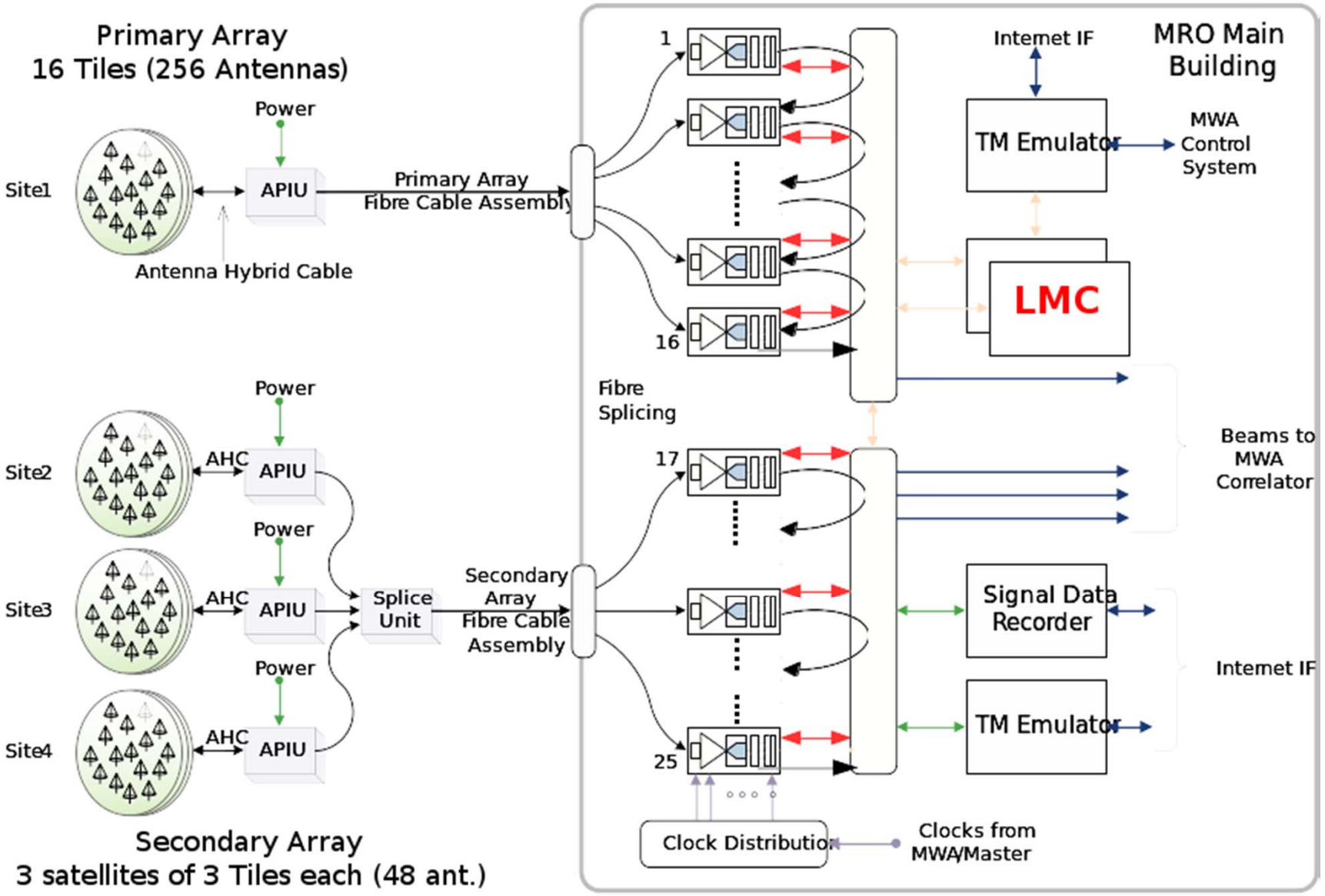

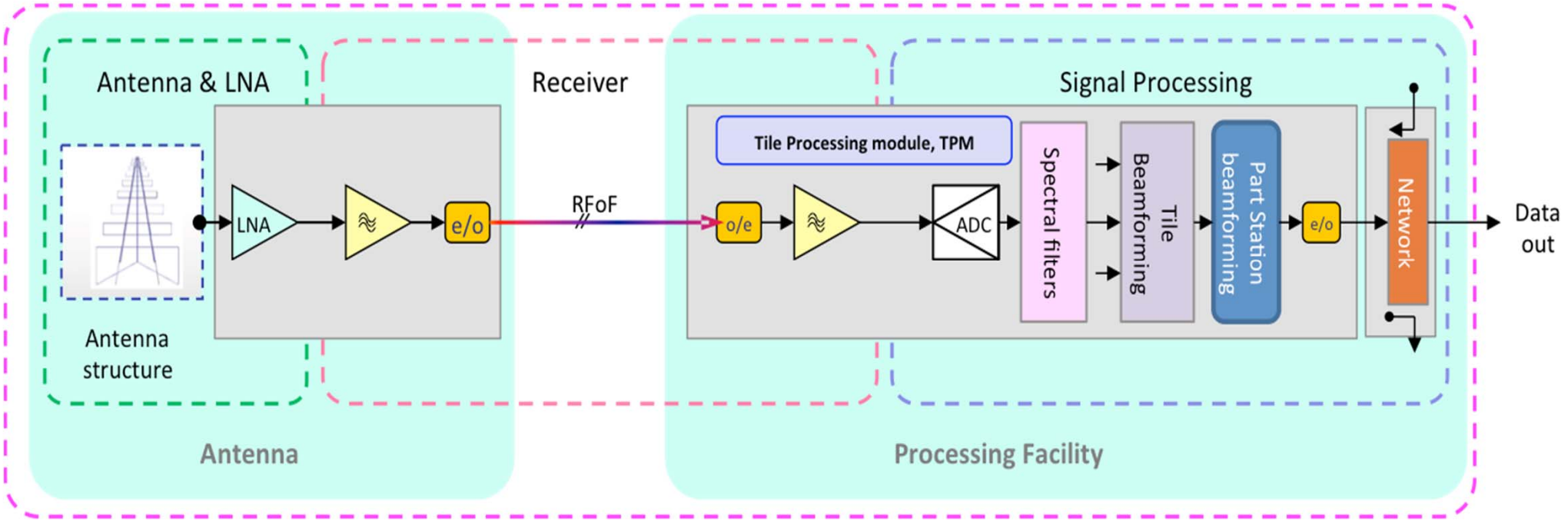

DAQ basic diagram

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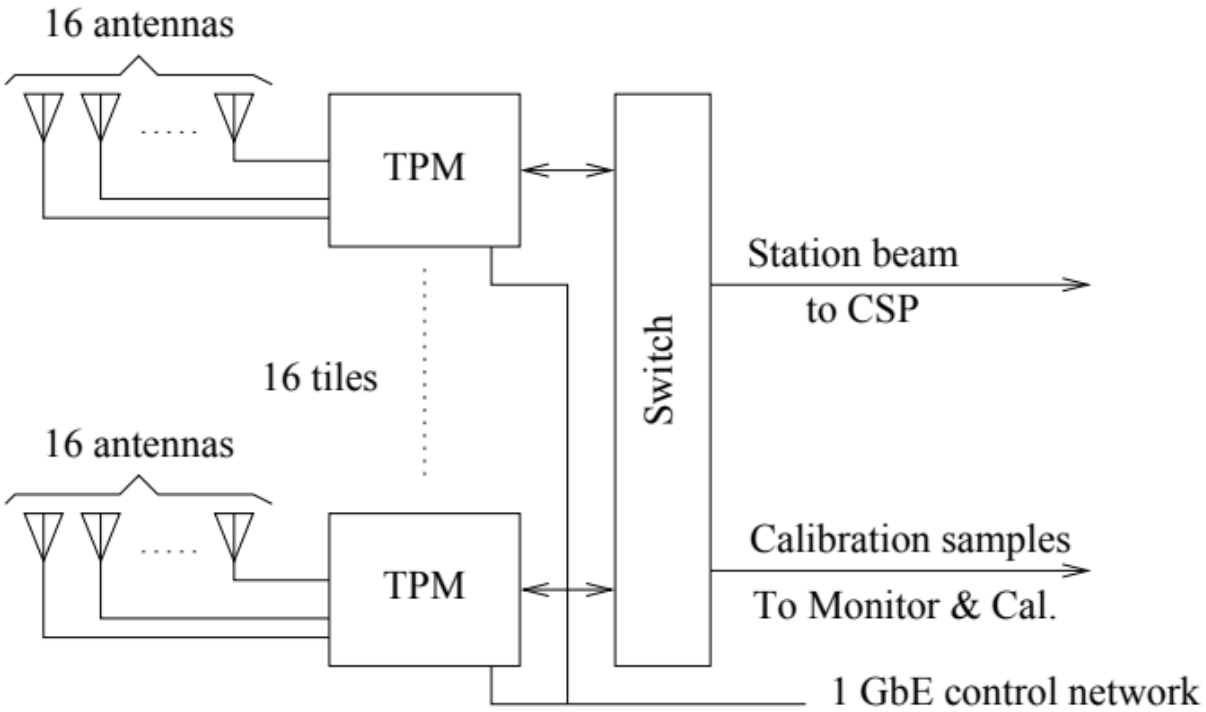

TANGO

SKA SQUARE KILOMETRE ARRAY CSP CENTRAL SIGNAL PROCESSOR

Central Signal Processor
Local Monitor and Control

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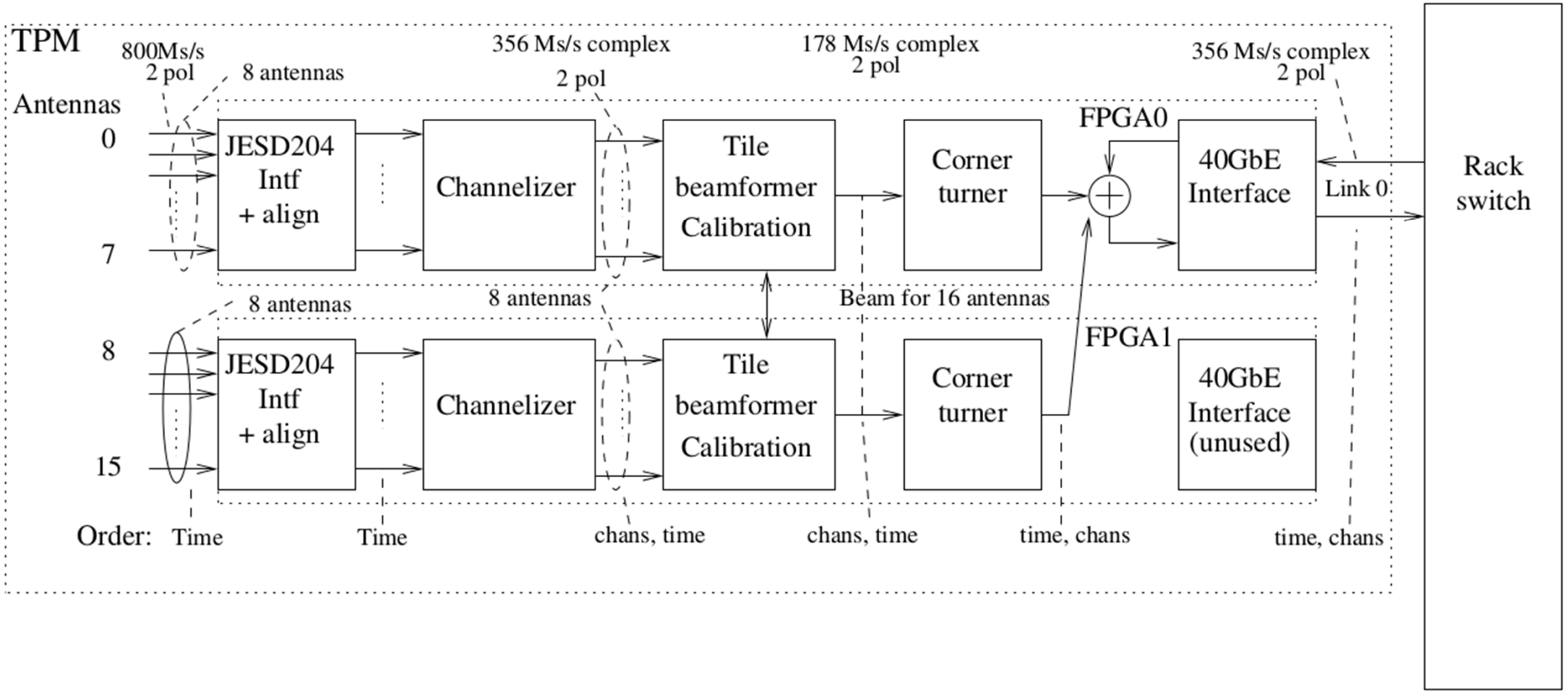

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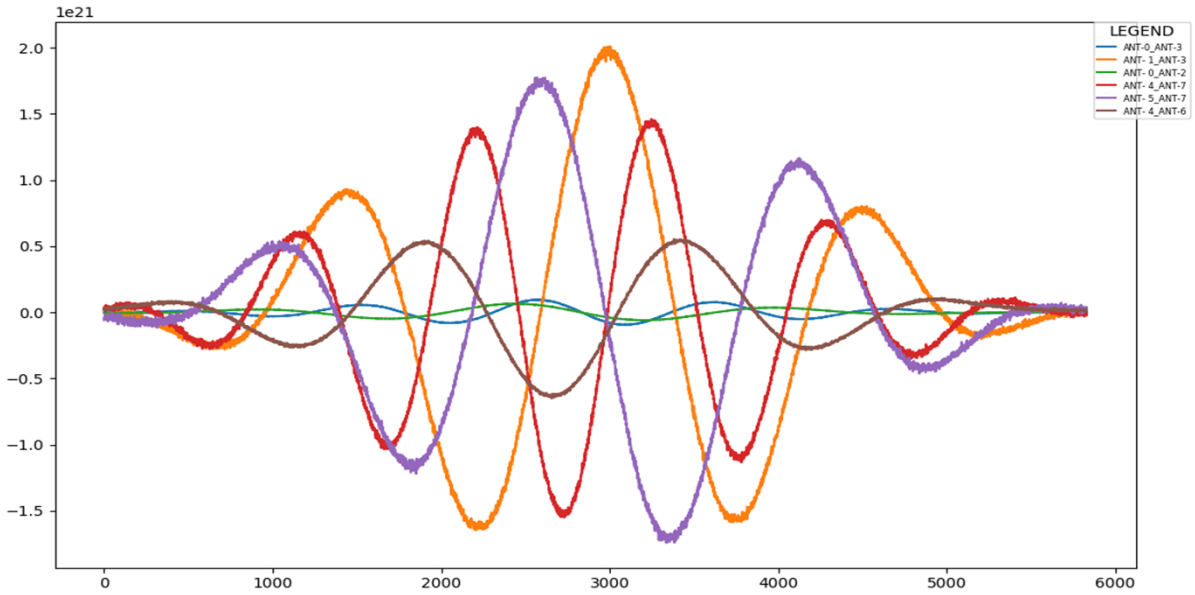
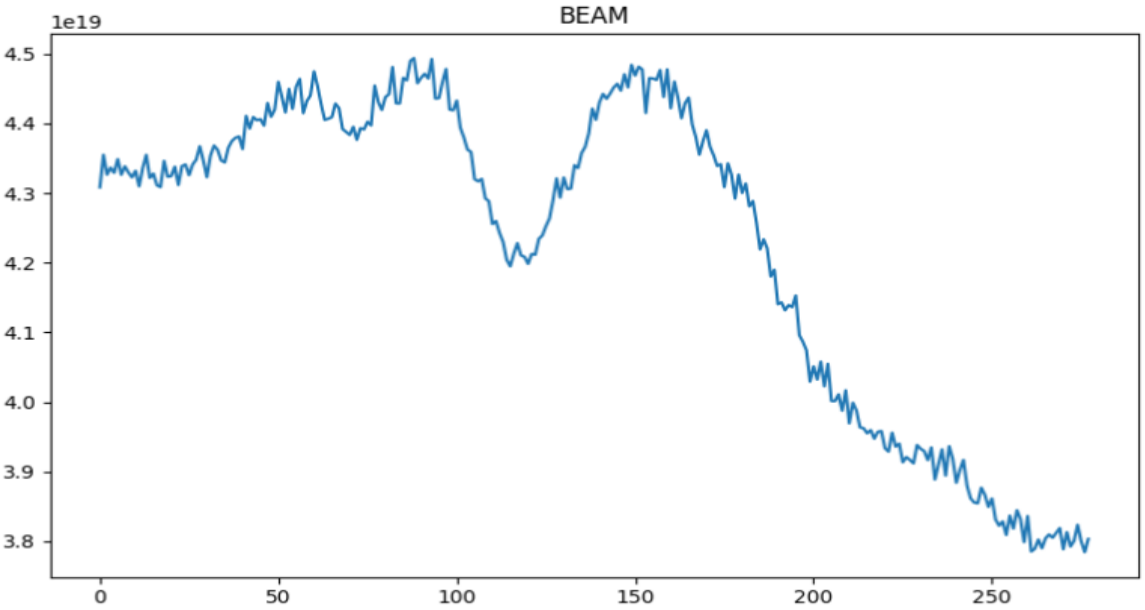


Coarse FFT channels Correlations



Tile not calibrated Beam

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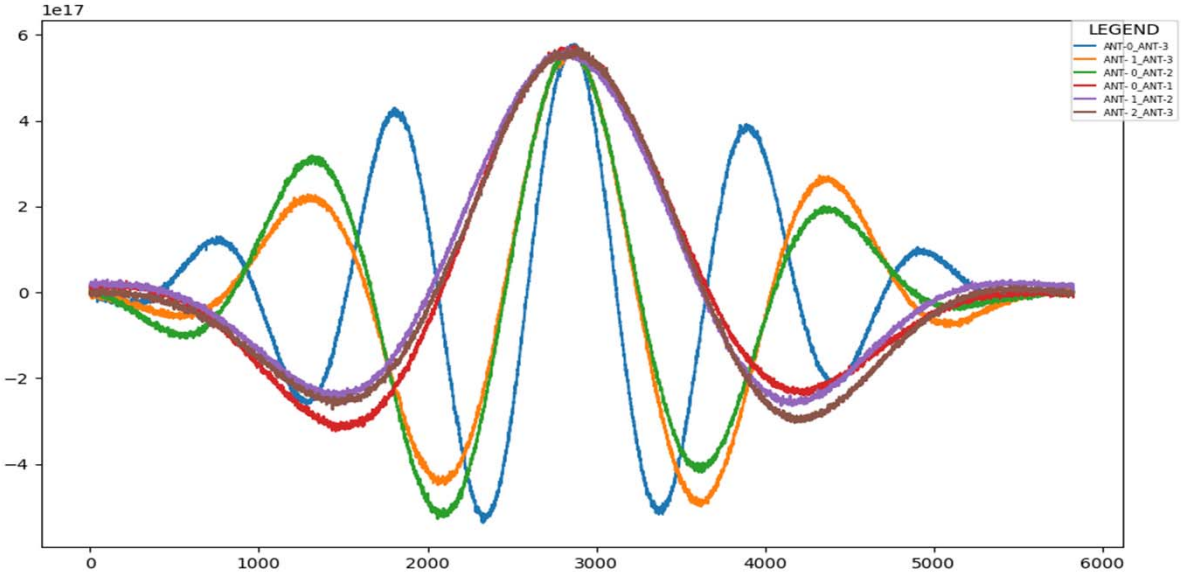
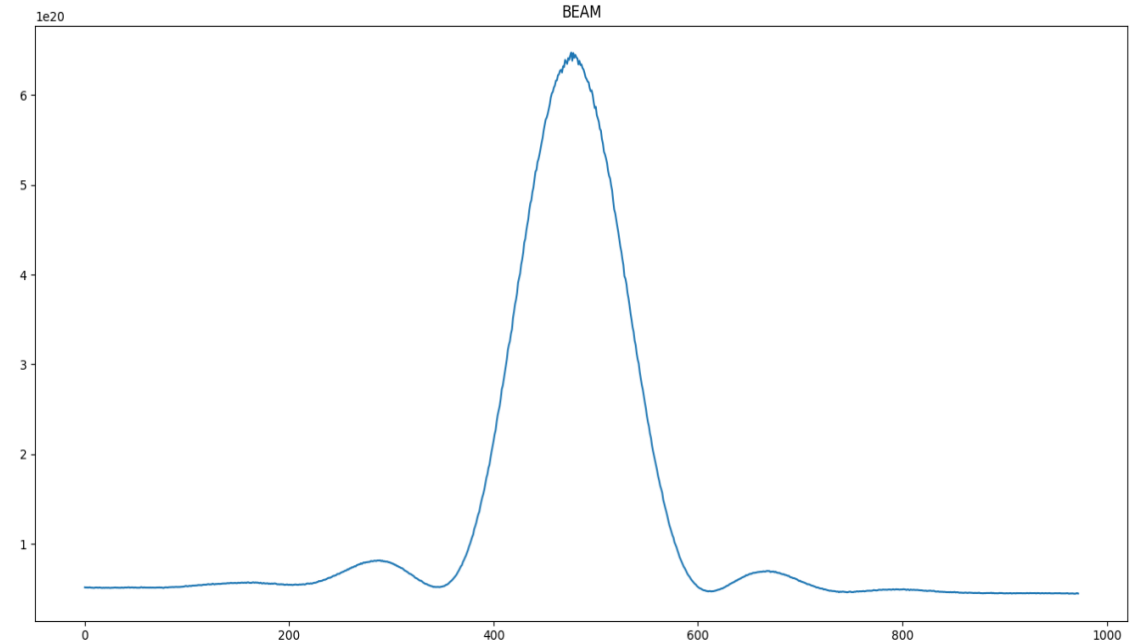
Phased FFT channels Correlations



Tile Calibrated Beam



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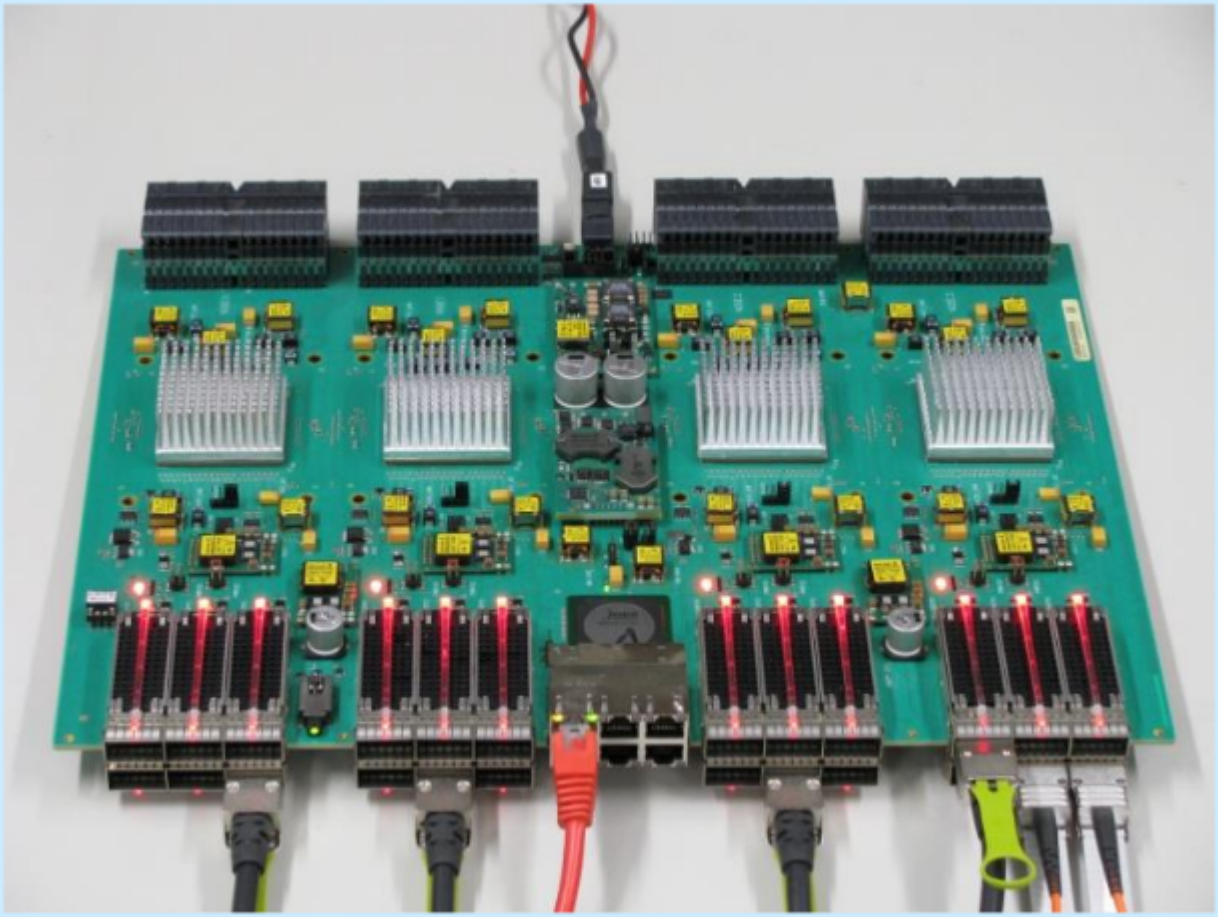
Uniboard2



Board specifications

IO:

- 24x QSFP+ 40GBASE for SR LR
- Backplane interface with:
- 192x 10GBASE interfaces
- 192x JESD204B ADC interfaces
- Total data throughput ~2Tbps

Environmental:

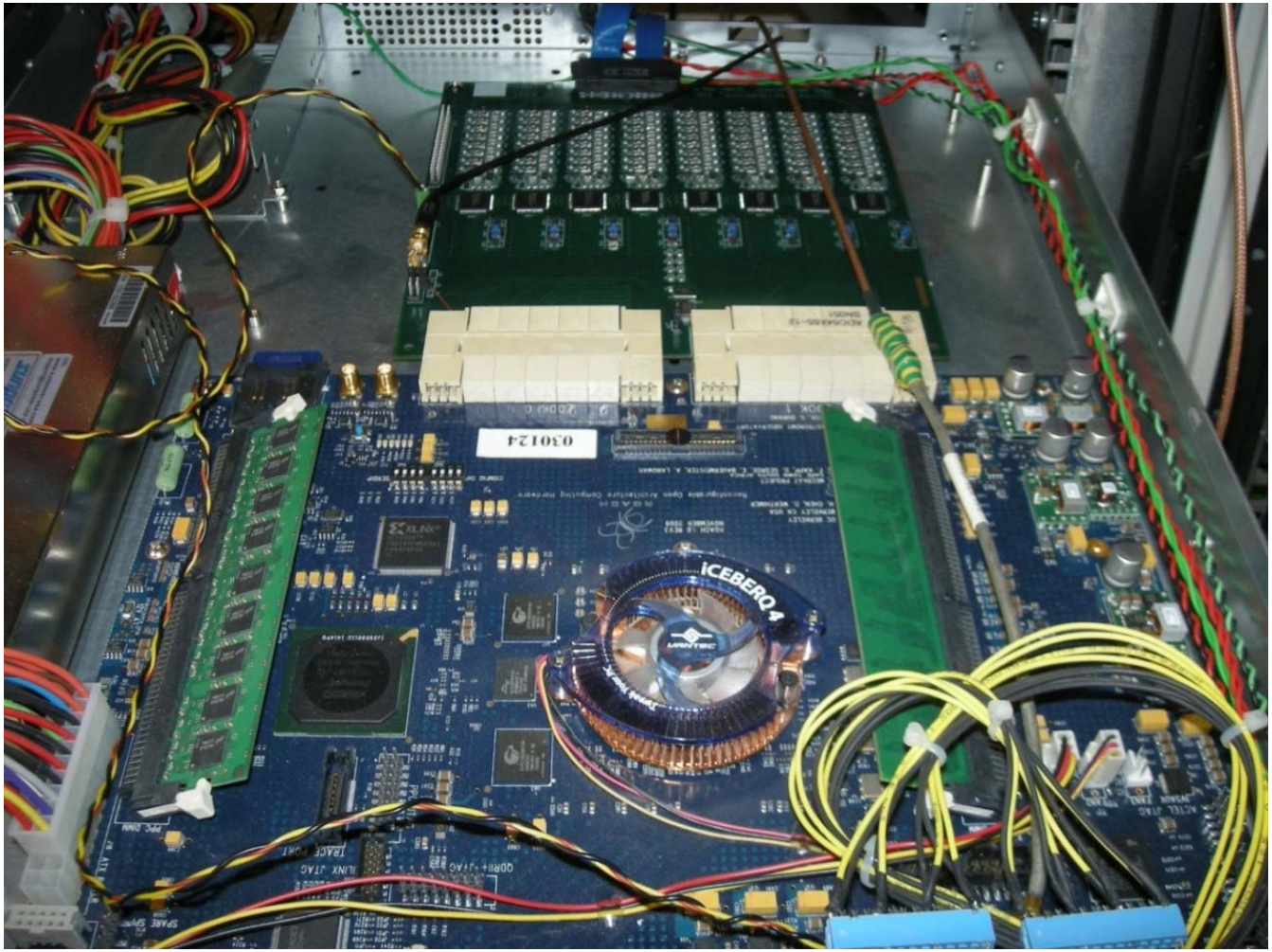
- Power supply: DC 48 V
- Power consumption: ~500 W
- Dimensions: 320 x 366 mm

ASTRON

RadioNet

SEVENTH FRAMEWORK PROGRAMME

ROACH + ADC64



64 Analog Inputs @ 40MSPS

Needs additional boards in cascade to compute full bandwidth correlations and beam-formers

Old FPGA Xilinx Families (Virtex-5 and Virtex-6)

THE UNIVERSITY OF CALIFORNIA BERKELEY 1868

CASPER

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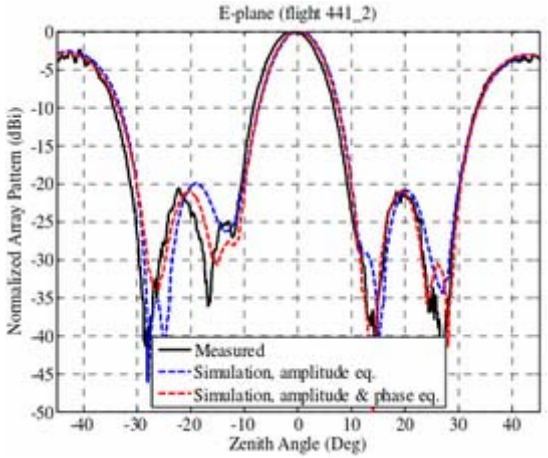
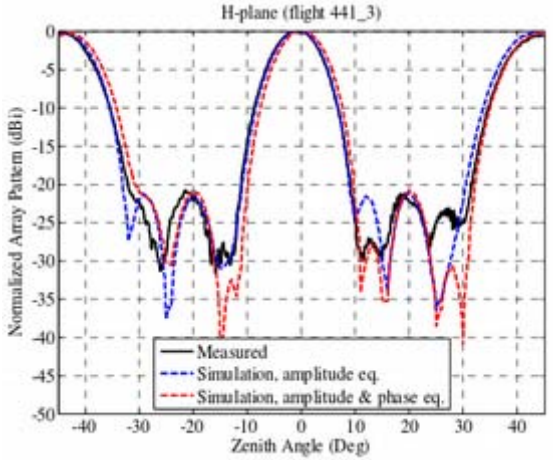
MAD Medicina Array Demonstrator

(9 Dual Polarizations Antennas, 3x3 regular spaced array)





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iTPM was born in May 2013, when was approved as **INAF Tecno** call for ideas:

"Digital Platform development for back end design of new generation SKA Aperture Arrays"

- 2 years program;
- financed by INAF with 161 k€.
- P.I. Francesco Schillirò (OACT)
- 5 INAF Institutes involved

Accepted as SKA project in *December 2013* inside *LFAA* Consortium

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iTPM

joint development teams

Sanitas EG
DIGITAL SYSTEMS, RESEARCH AND INNOVATION

CAMPERA electronic systems

LighTech
Fiber Optics Components and Accessories

OPTEL
OPTOELETTRONICA TELECOMUNICAZIONI

UNIVERSITY OF OXFORD

ees
ELECTRONIC ENGINEERING SERVICE

RGM

XILINX
ALL PROGRAMMABLE™

ANALOG DEVICES

Selex ES
A Finmeccanica Co

Microwavefilters & tvc
Microwave components for telecommunication systems
Alongside our customers in the telecommunication market since 1979

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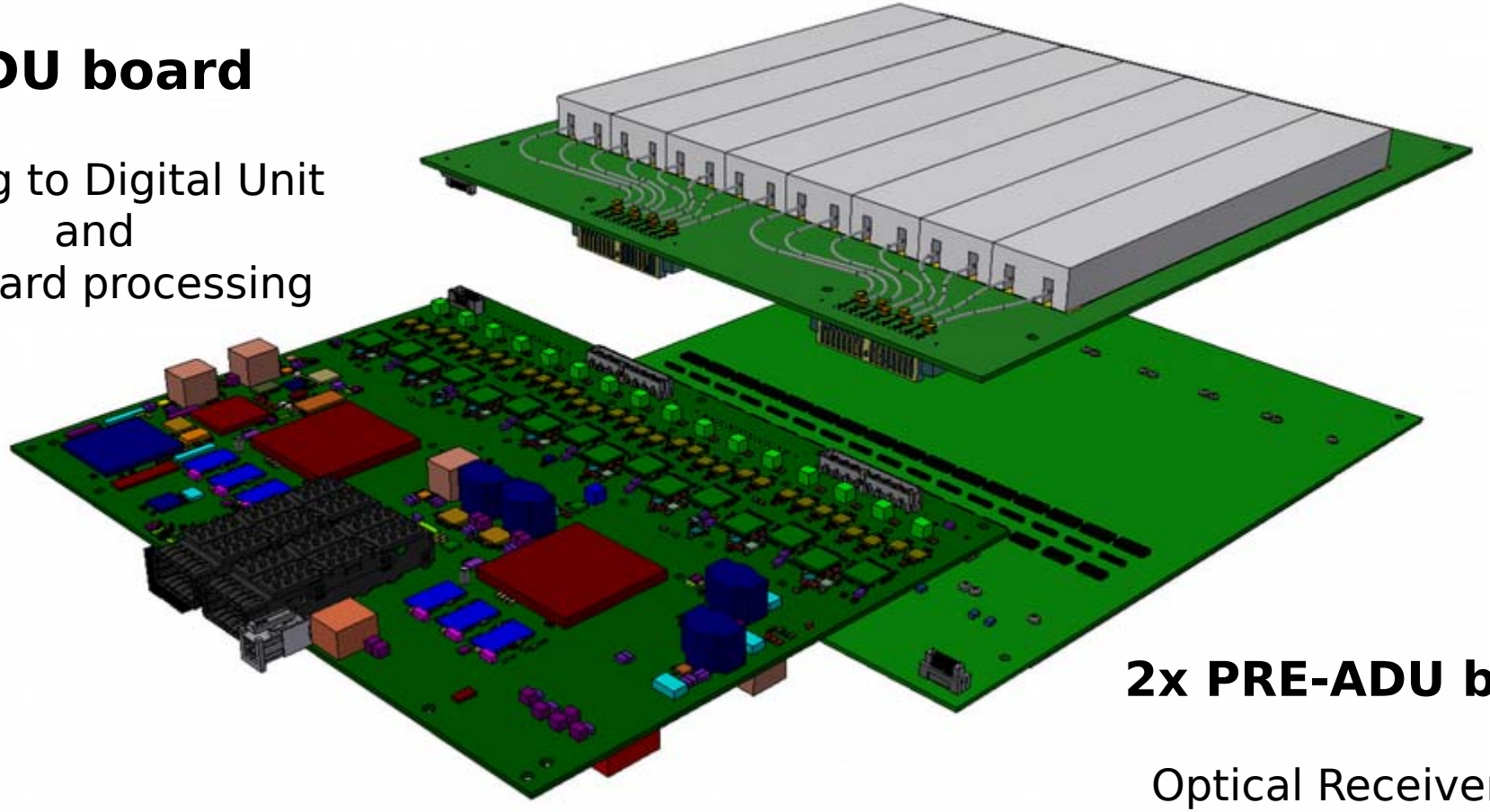
ADU board

Analog to Digital Unit
and
on-board processing



2x PRE-ADU boards

Optical Receivers and
signal conditioning

iTPM modules

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440.5 mm depth

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6U x 21hp format (4 iTPMs fit 19 inches SubRack)

4x Quad LC connectors for the 16 optical inputs

1x RJ45 Gigabit port for the Management

2x 40Gb QSFP+ ports

1x supply socket

1x SMA input for 10MHz Reference signal

1x SMA input for PPS Sync signal

ITPM Front Panel

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PRE-ADU board

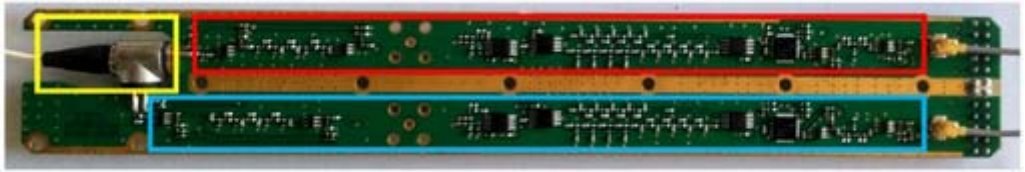
A set of **8 Optical RX** using **WDM** technology
(two optical wavelength transmitted in one fiber)

SPI Registers Lane for Signal Conditioning configuration

Optical Receiver

2 Selectable Filters:
375 MHz (low pass)
375-650 MHz (pass band)

31.5 dB digital step attenuators
(0.5 dB resolution)



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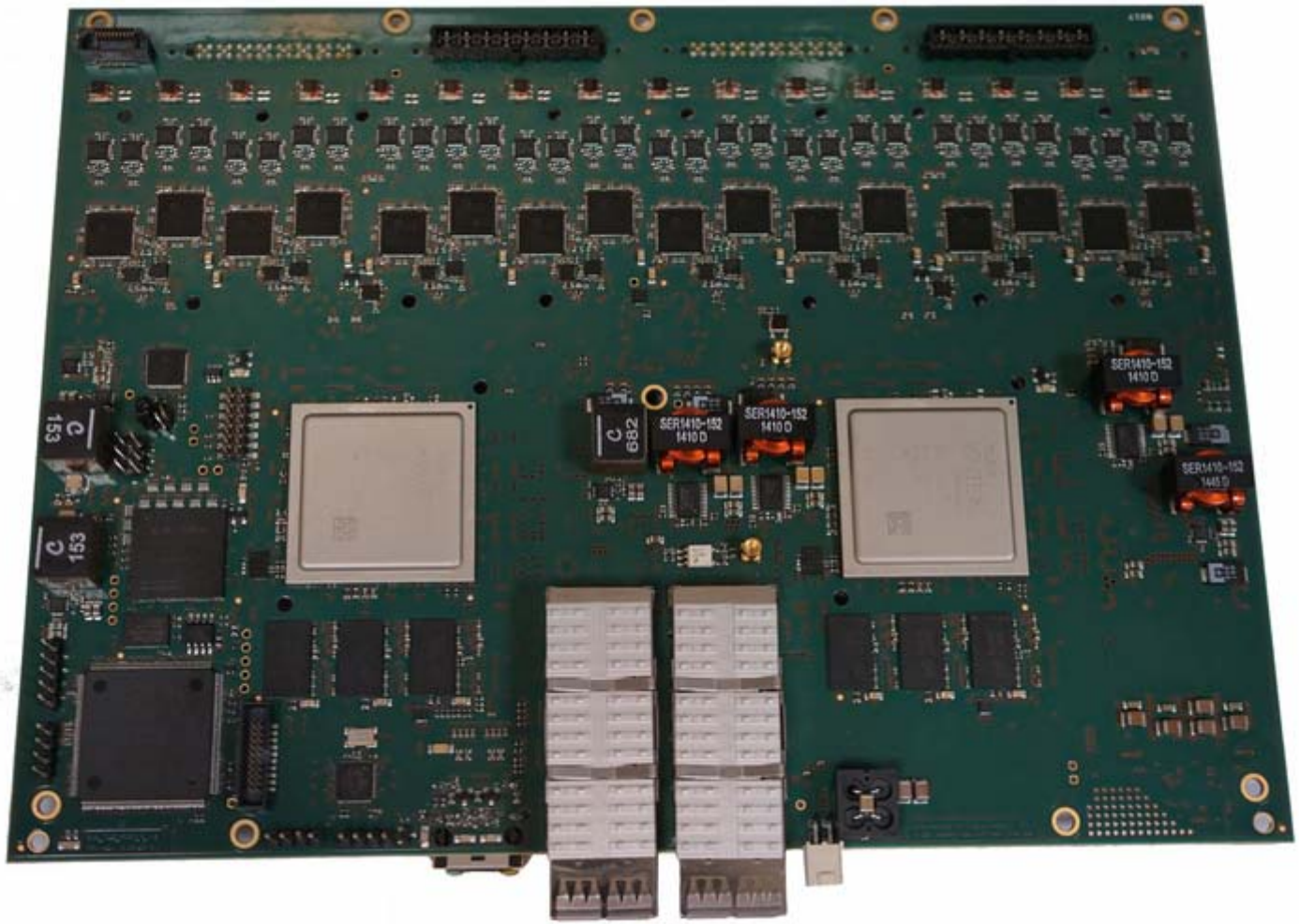

ADU board top view

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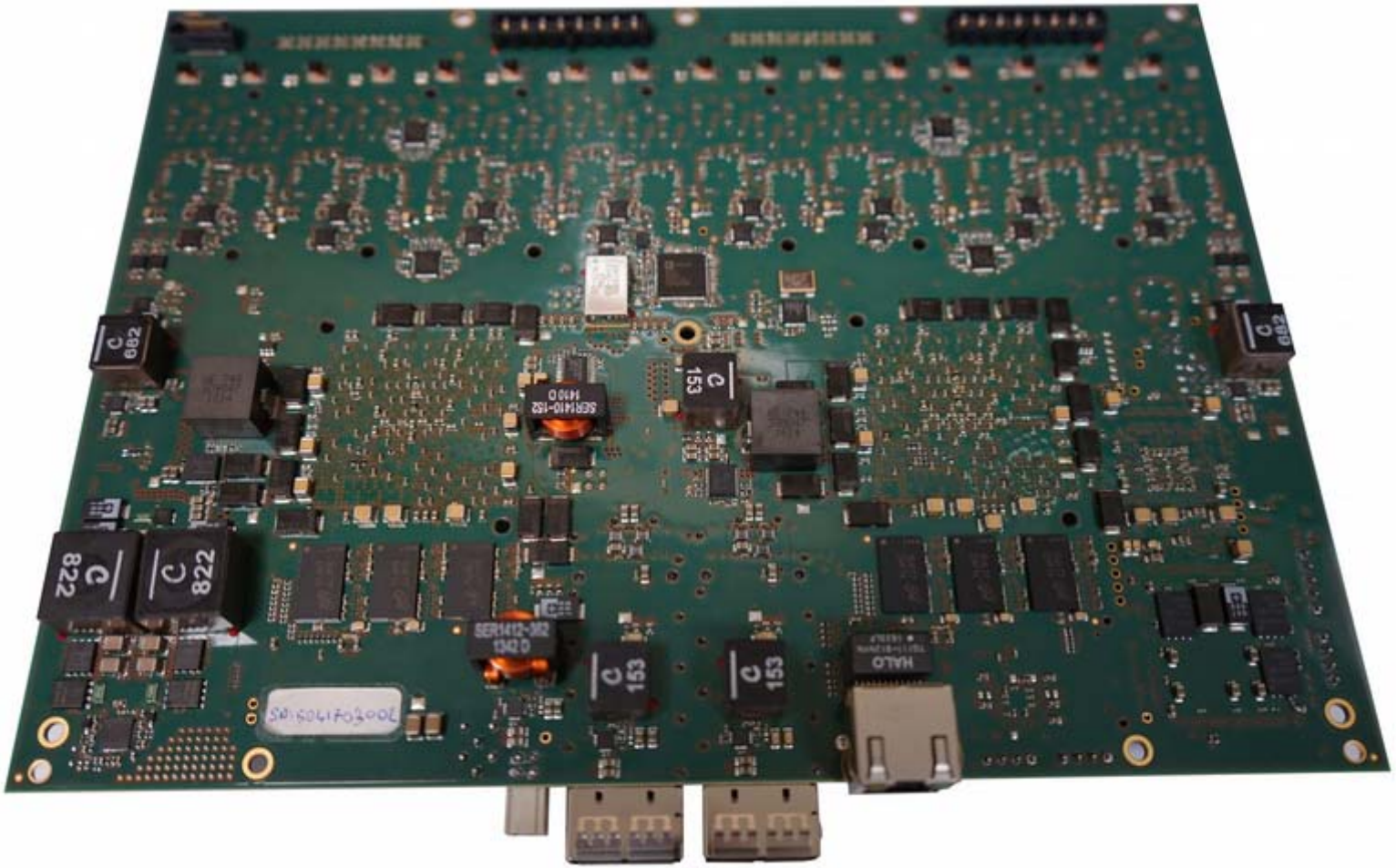

ADU board bottom view

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DAQ stage

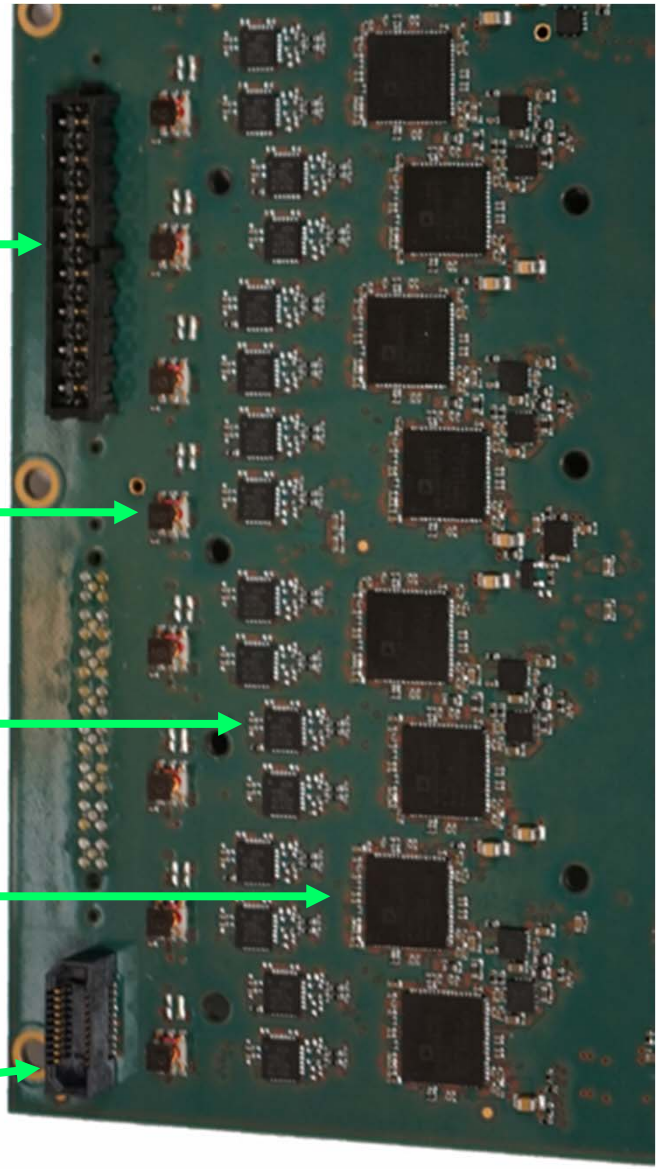
4x SAMTECH connectors for 8 single ended RF input signals each

32x Single ended to differential balun converters

32x High performance BiCMOS RF digital gain amplifiers

16x Dual 14-bit, 1.25 GSPS Analog to digital converters
JESD204B-based high speed serialized output

PRE-ADU supply and SPI bus



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Kintex® UltraScale™ FPGAs

	Device Name	KU025[1]	KU035	KU040	KU060	KU085	KU095	KU115
Logic Resources	System Logic Cells (K)	318	444	530	726	1,088	1,176	1,451
	CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
	CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	4,230	5,908	7,050	9,180	13,770	4,800	18,360
	Block RAM/FIFO w/ECC (36Kb each)	360	540	600	1,080	1,620	1,680	2,160
	Block RAM/FIFO (18Kb each)	720	1,080	1,200	2,160	3,240	3,360	4,320
	Total Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
	I/O DLL	24	40	40	48	56	64	64
I/O Resources	Maximum Single-Ended HP I/Os	208	416	416	520	572	650	676
	Maximum Differential HP I/O Pairs	96	192	192	240	264	288	312
	Maximum Single-Ended HR I/Os	104	104	104	104	104	52	156
	Maximum Differential HR I/O Pairs	48	48	48	48	56	24	72
Integrated IP Resources	DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
	System Monitor	1	1	1	1	2	1	2
	PCIe® Gen1/2/3	1	2	3	3	4	4	6
	Interlaken	0	0	0	0	0	2	0
	100G Ethernet	0	0	0	0	0	2	0
	16.3Gb/s Transceivers (GTH/GTY)	12	16	20	32	56	64[2]	64
Speed Grades	Commercial	-1	-1	-1	-1	-1	-1	-1
	Extended	-2	-2 -3	-2 -3	-2 -3	-2 -3	-2	-2 -3
	Industrial	-1 -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -2	-1 -1L -2

	Package Footprint[3, 4, 5, 6]	Package Dimensions (mm)	HR I/O, HP I/O, GTH/GTY					
Footprint Compatible with Virtex® UltraScale Devices	A784[7]	23x23[8]		104, 364, 8	104, 364, 8			
	A676[7]	27x27		104, 208, 16	104, 208, 16			
	A900[7]	31x31		104, 364, 16	104, 364, 16			
	A1156	35x35	104, 208, 12	104, 416, 16	104, 416, 20	104, 416, 28		52, 468, 28	
	A1517	40x40				104, 520, 32	104, 520, 48		104, 520, 48
	C1517	40x40						52, 468, 40	
	D1517	40x40							104, 234, 64
	B1760	42.5x42.5					104, 572, 44	52, 650, 48	104, 598, 52
	A2104	47.5x47.5							156, 676, 52
	B2104	47.5x47.5						52, 650, 64	104, 598, 64
	D1924	45x45							156, 676, 52
	F1924	45x45					104, 520, 56		104, 624, 64

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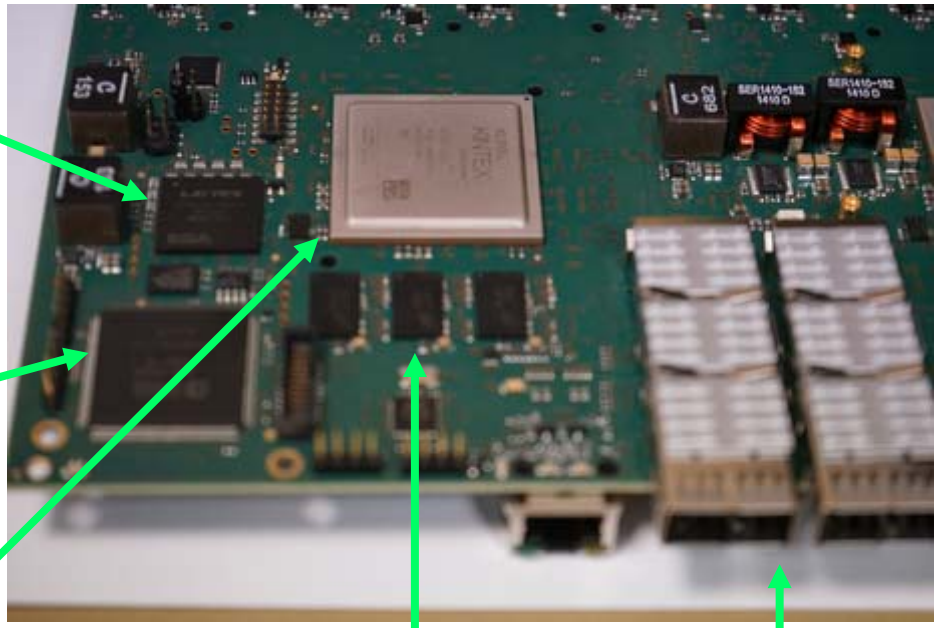
Low-level Ethernet gigabit management interface with instant ON flash based Lattice CPLD

On board tree 256Mbit SPI user flash for multiple FPGA configuration options

Second level management microprocessor (ARM Cortex A8, 32 bit, 240 MHz) for high-level remote board control



2x Xilinx Kintex Ultrascale FPGAs

- GTX receivers for the MultiGigabit link (JESD204B)
- 16.3Gb/s Transceivers (GTH/GTY) for QSFP+

Two DDR3, 96 bit memory banks, 6+6 Gbit total size

High speed internal bus to connect the 2 FPGAs, 25 Gbit/s + 25 Gbit/s bidirectional

2x 40Gb QSFP+ Links

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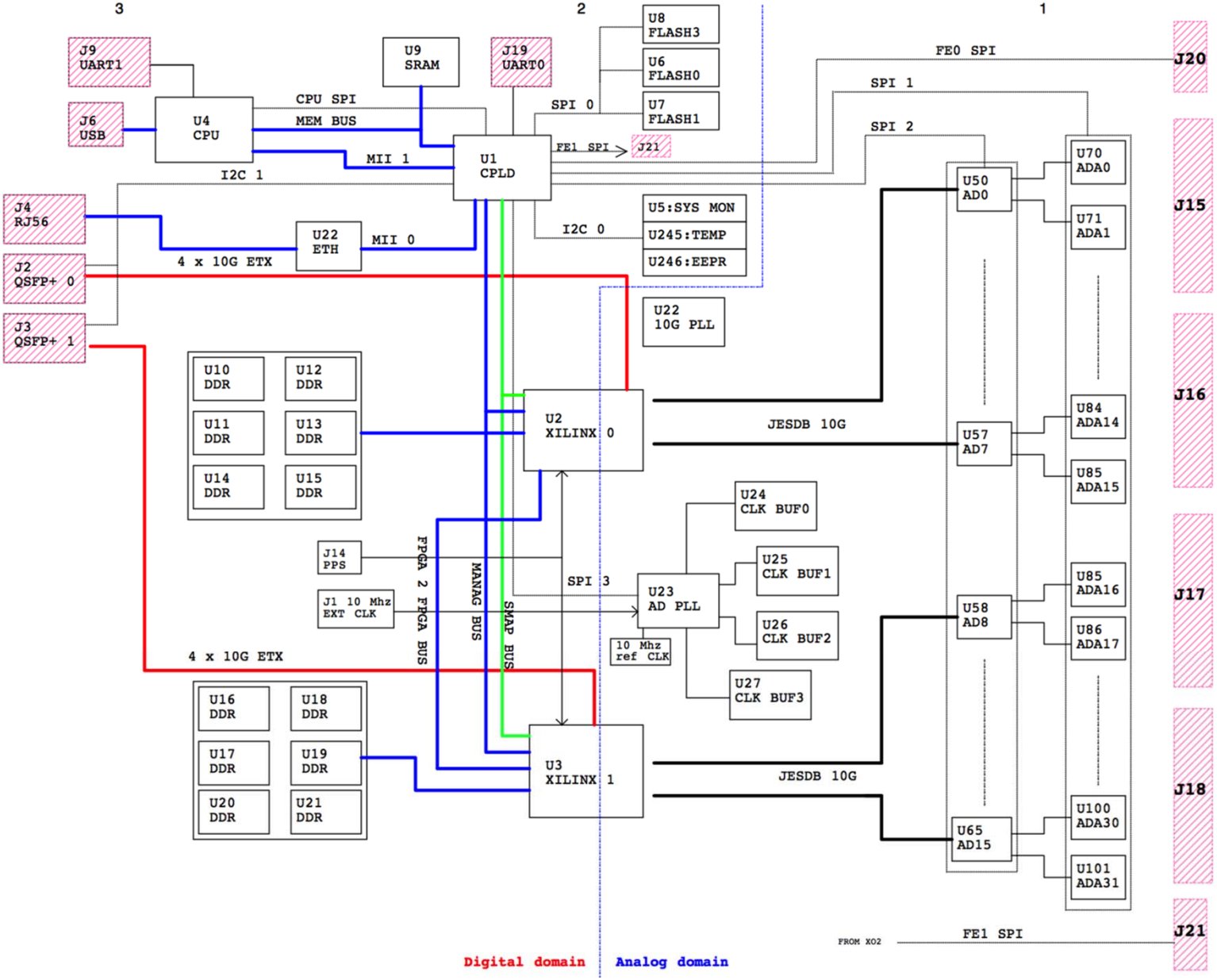


iTPM Station Beamformer Firmware

- ADCs sample 14 bit @ 800MSPS and send 8 most significant bit to FPGAs

- Polyphase Filter Bank FFTs of 781.25KHz resolution (512 freq. Channels)

- Apply Calibration coefficients

- Compute Tile Beam, add the Beam of the previous Tile and send the result to the next TPM via 40Gb link

ADU Test Firmware

- ADCs sample 14 bit @ 800MSPS and send 8 most significant bit to FPGAs

- CPLD collect 2MB buffer per FPGA and send time domain data using UDP Packets via the Gigabit link

ADU Performance Measurements

A set of frequencies spanning in the range 50 ÷ 400 MHz was selected

The Workstation controls the Signal generator and the Power Meter via GPIB

The Workstation sets frequencies to the Signal Generator and corrects the amplitudes by reading the level with a Power Meter or Spectrum Analyzer.

Therefore the ADU board inputs have always a constant level over the bandwidth of about -1 dBFS.

ADU board stores time domain data in a 2MB BRAM and sends UDP packets continuously through 1Gbit Ethernet

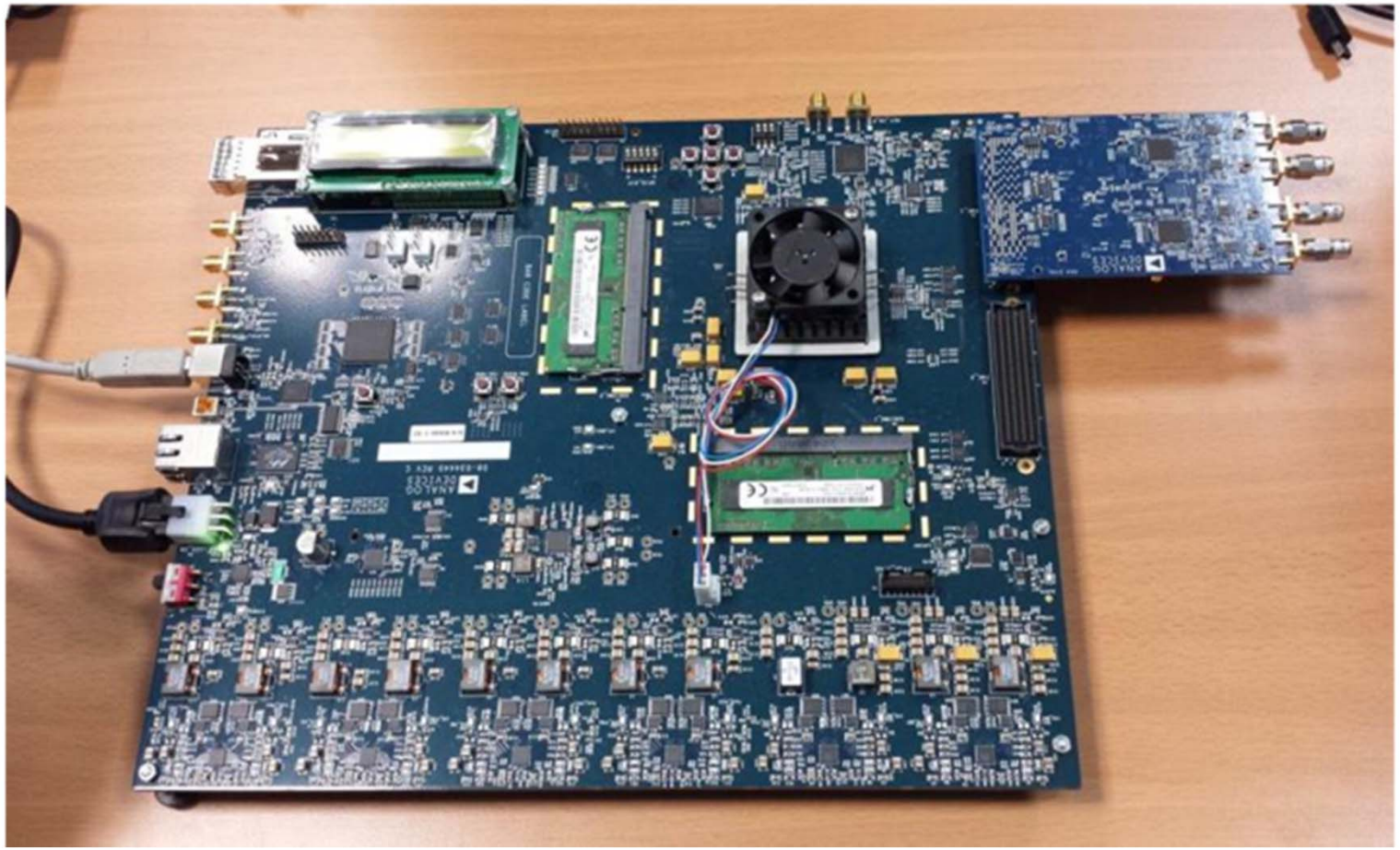
The workstation gets UDP packets and saves files using Python Script

Matlab routines process data (FFT) and compute some ADC parameters to evaluate the performance over the bandwidth (SNR, SFDR, SINAD, ENOB, etc…).

Analog Device

ADS7-V1EBZ FPGA Based Data Capture Kit

Feature: Based on Virtex-7 FPGA, Two (2) FMC-HPC connectors, Ten (10) 13.1 Gbps transceivers per FMC-HPC connector, Two (2) DDR3-1866 DIMMs, Simple USB port interface (2.0)



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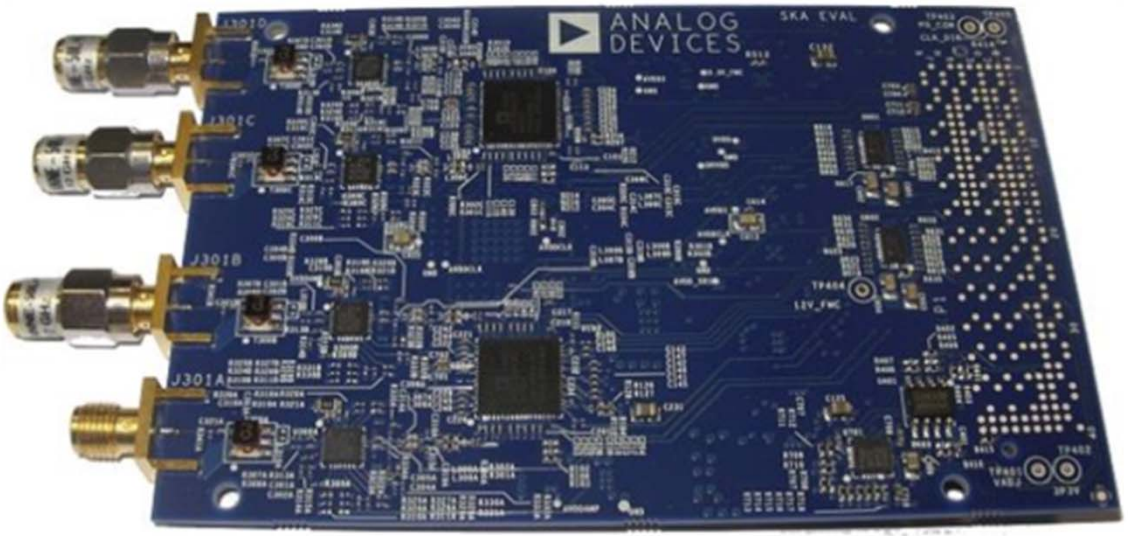
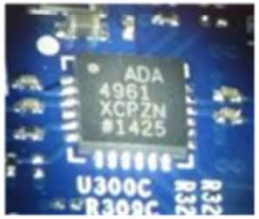
Analog Device

SKA EVAL AD-FMCADC4-EBZ



TCM2-43X+

Mini-Circuits Balun
RF Transformer 50Ω



ADA4961

Low Distortion Amplifier
3.2 GHz, RF DGA

AD9234

12-Bit, 1 GSPS/500 MSPS JESD204B
Dual Analog-to-Digital Converter

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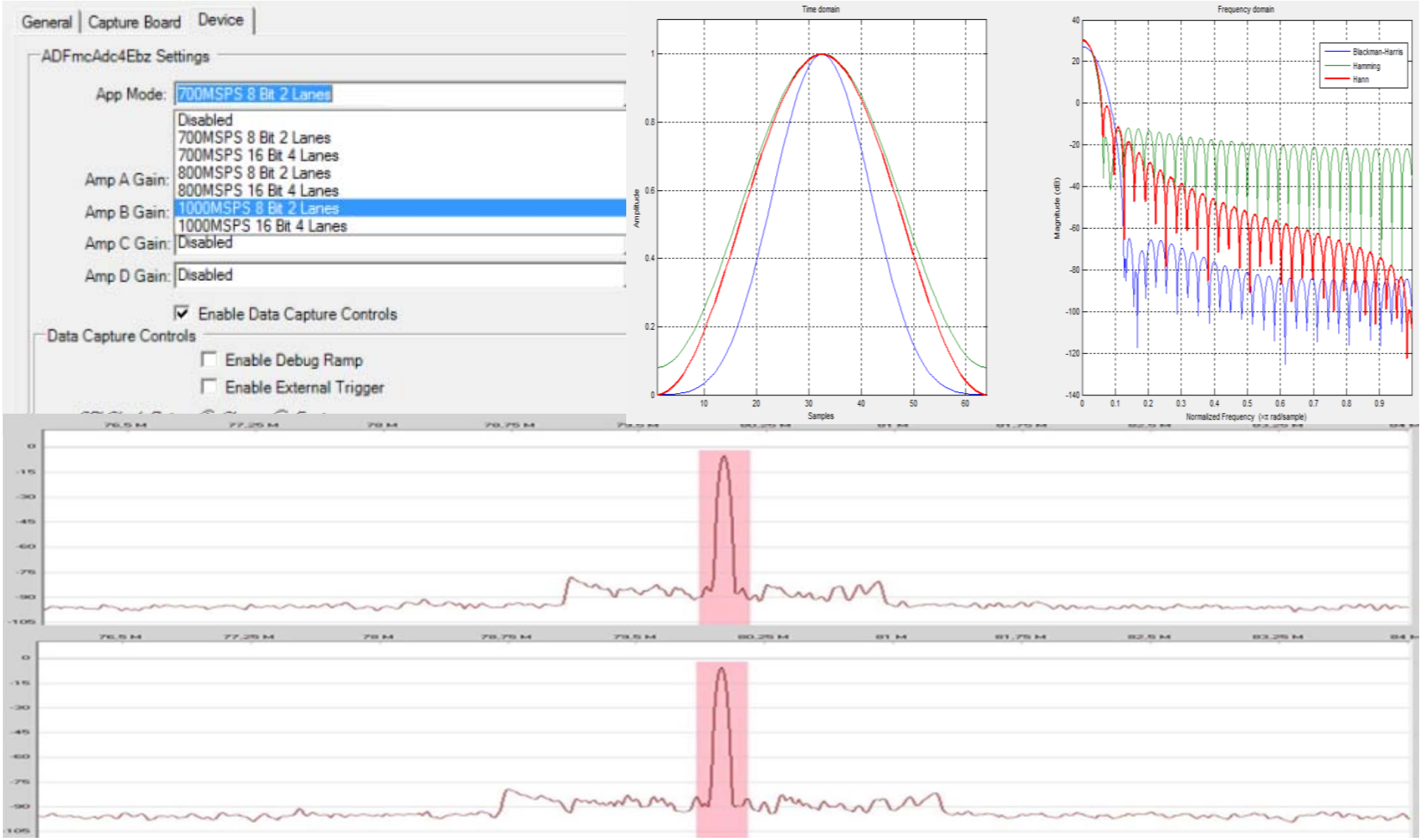

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Lock everything to ultra stable 10 MHz reference

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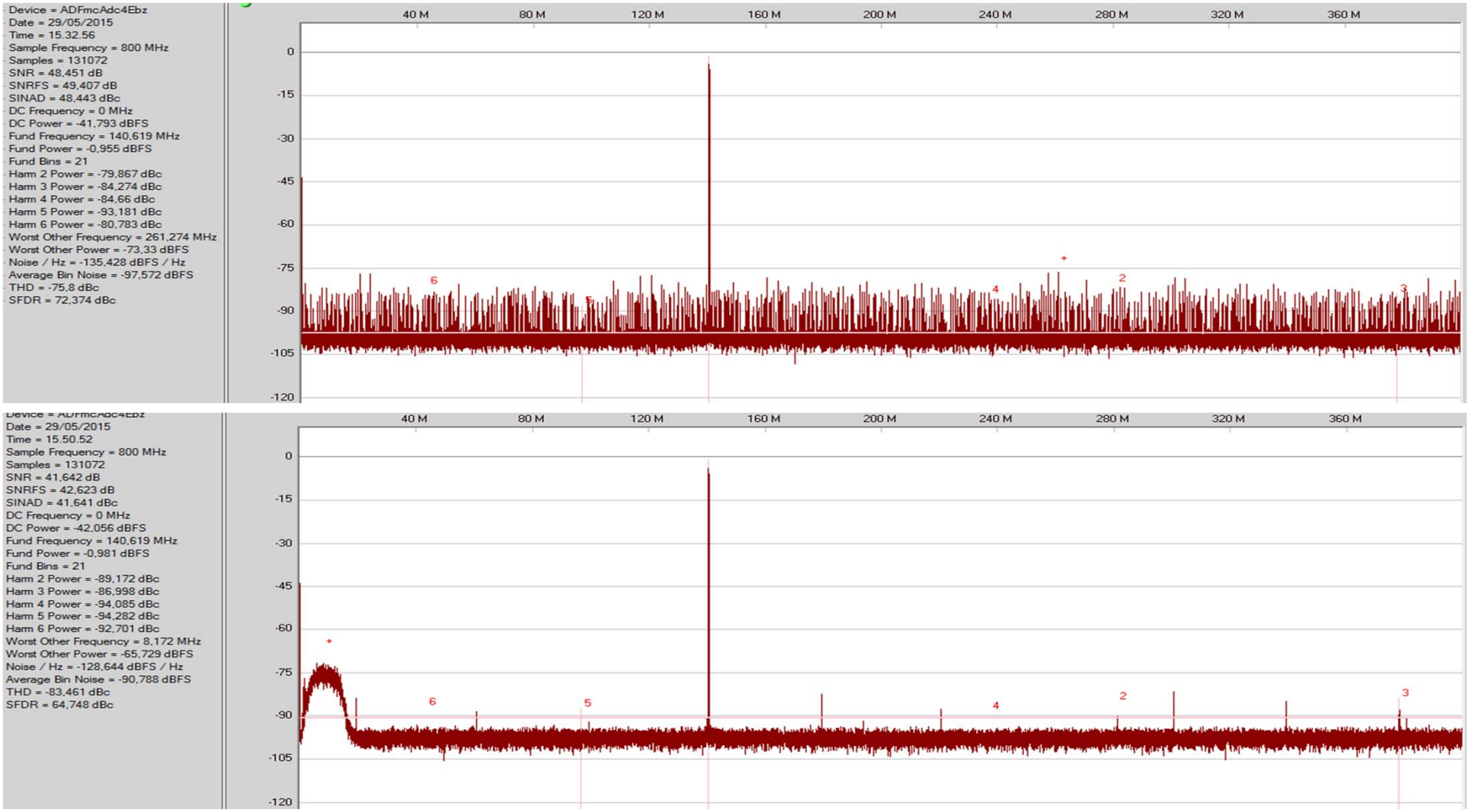
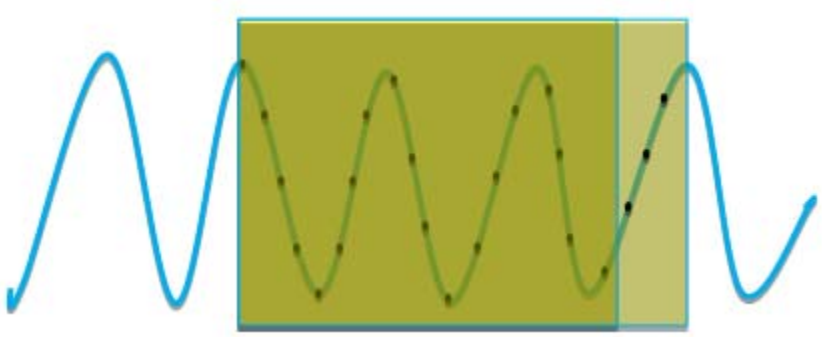


Dithering may improve quality of measurements but increase the noise floor

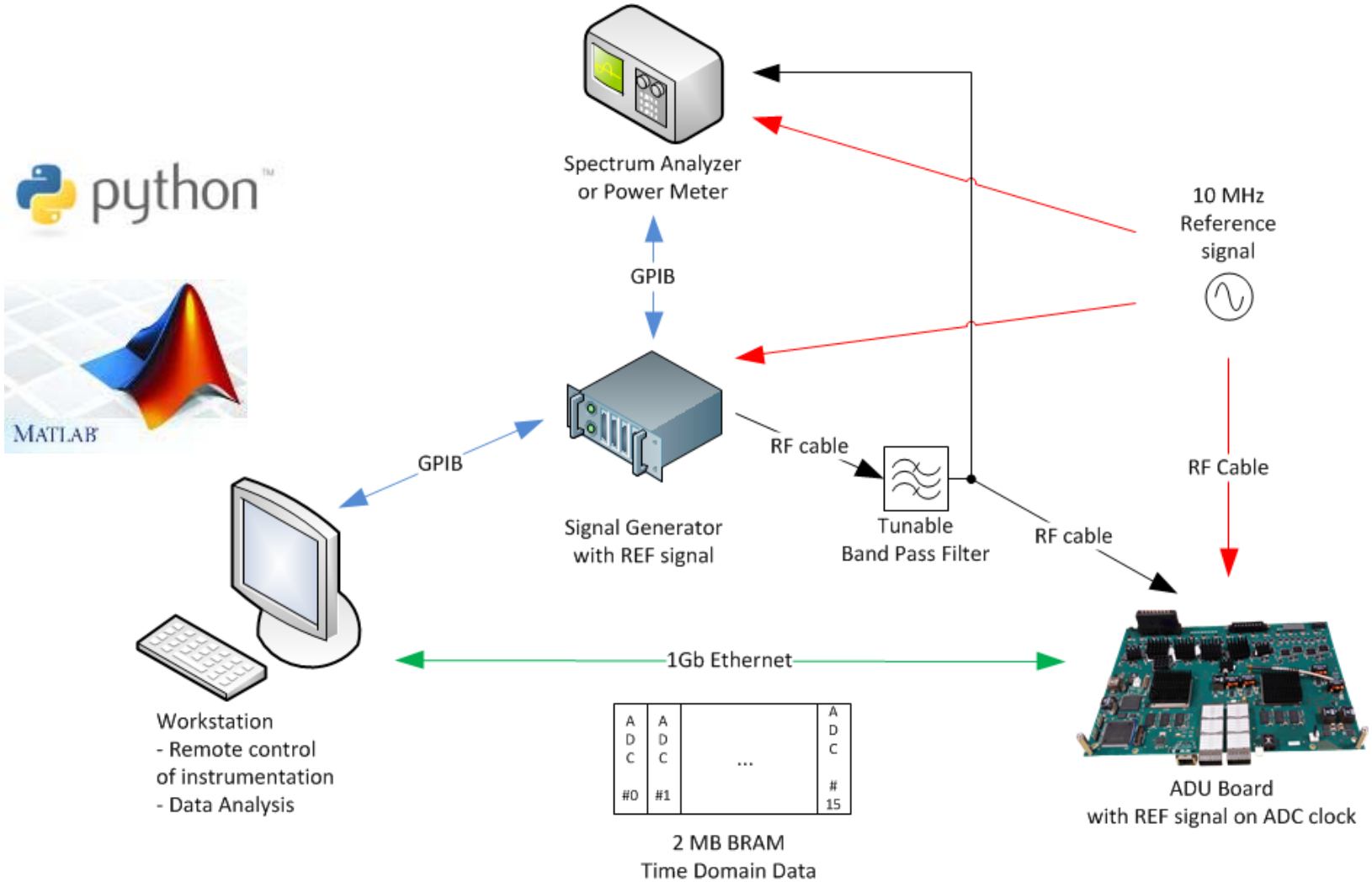
Working with monochromatic signals directly injected to an ADC converter may be a very hard work The Fast Fourier Transform may show “unreal” results

Selection of the frequency

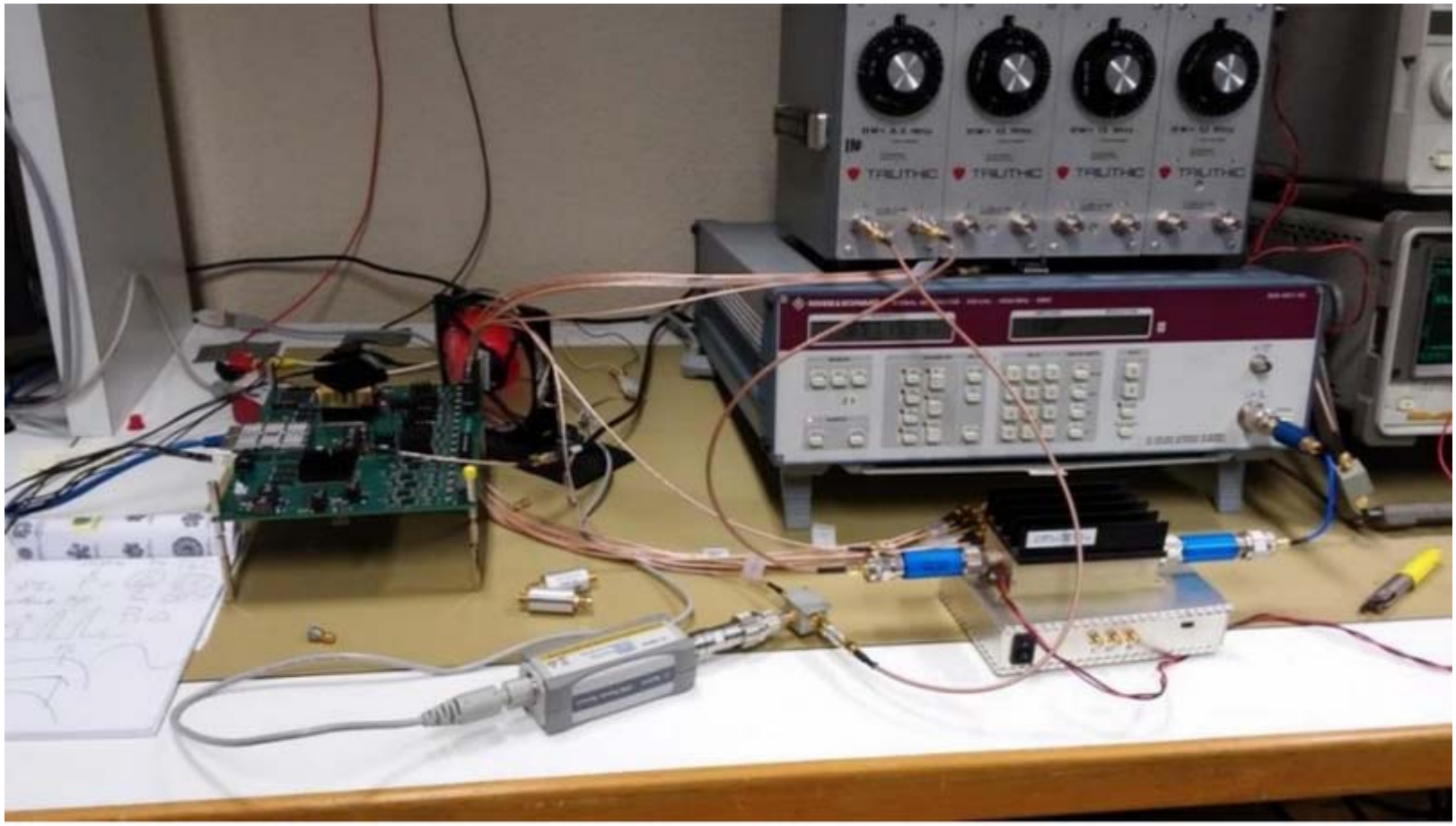


$$Cycles = \frac{f_{DESIRED\_FREQUENCY}}{\frac{Sample\_Rate}{FFT\_Samples}}$$

Bibliography: Understanding High Speed ADC Testing and Evaluation, AN-835 Application Note, Rev. B, by Alex Arrants, Brad Brannon and Rob Reeder



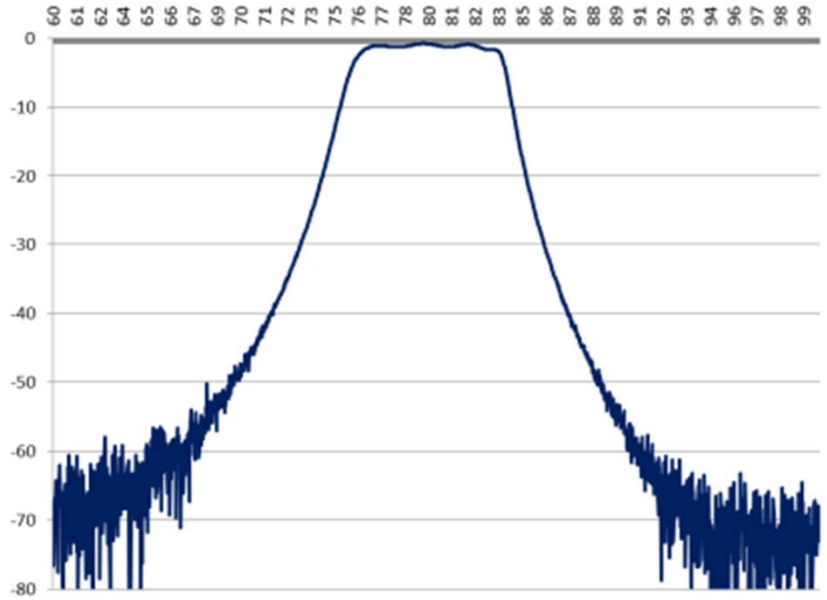
ADU Test Setup



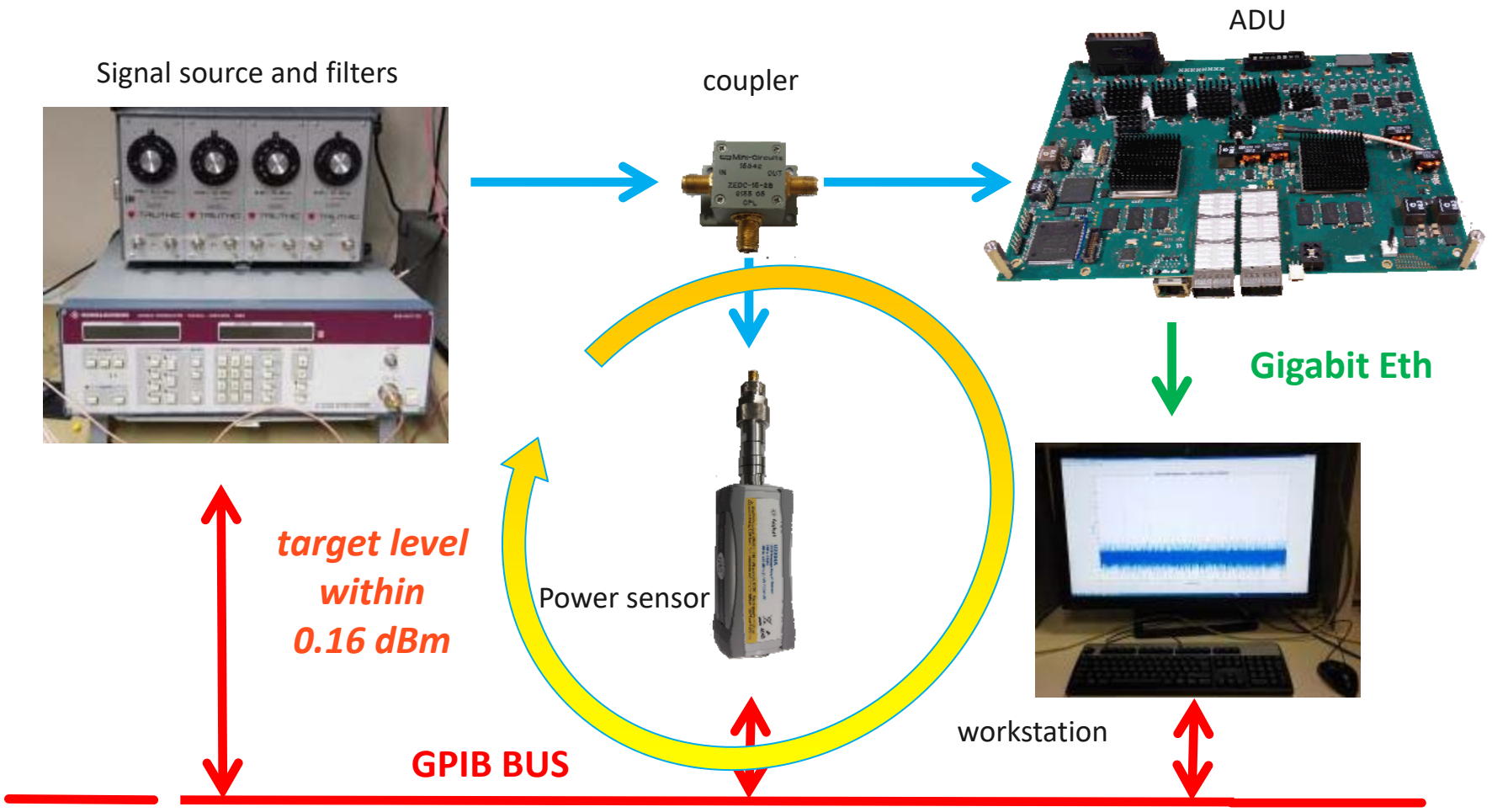
ADU Test Setup

Tunable Bandpass Filter

- Bandwidth depends on the filter bank
- Filter response depends on the tuning
- No remote control available

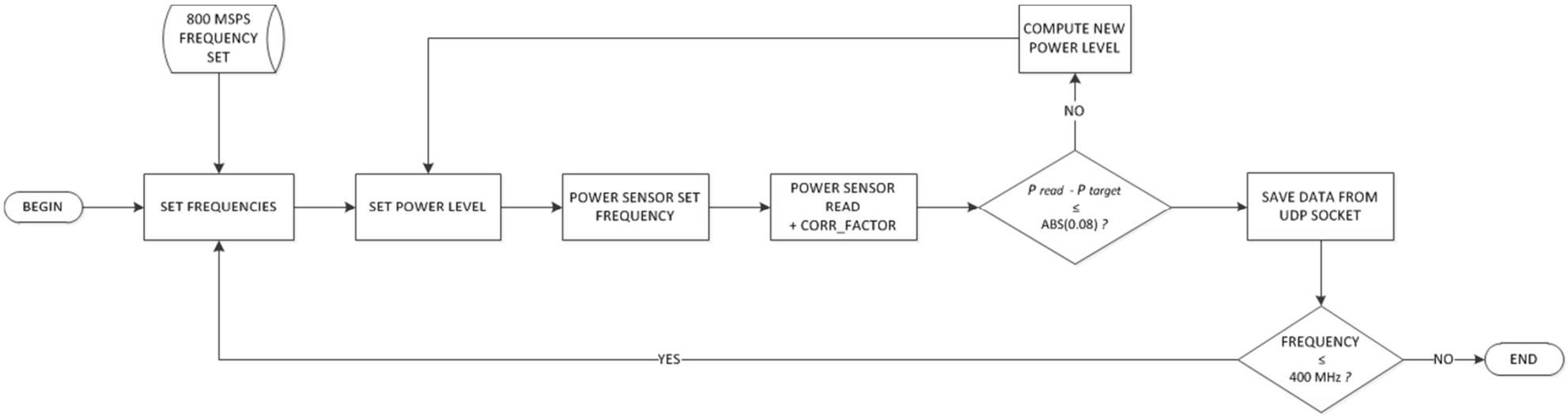


ADU Test Setup



ADU Test Setup

Process Controller



ADU Test Setup

```
D:\SKA-TPM\PythonScript\sdp>python adc_tpm_cal.py -i 4 -n 10
CPL Correction Factor Enabled

Opening GPIB devives...
Found Signal Generator ROHDE&SCHWARZ SMX on GPIB Addr 25

Select a Frequencies file...
Opening file: D:\SKA-TPM\Freqs\SLP100_freqfile_50-100_800_131072.txt
Found 65 frequencies!

[1/65]  Freq: 53143310 Hz, Acq # 10/10
[2/65]  Freq: 53900140 Hz, Acq # 10/10
[3/65]  Freq: 54632560 Hz, Acq # 10/10
[4/65]  Freq: 55340570 Hz, Acq # 10/10
[5/65]  Freq: 56146240 Hz, Acq # 10/10
[6/65]  Freq: 56878660 Hz, Acq # 10/10
[7/65]  Freq: 57611080 Hz, Acq # 10/10
[8/65]  Freq: 58294670 Hz, Acq # 10/10
[9/65]  Freq: 59136960 Hz, Acq # 10/10
[10/65]  Freq: 59881590 Hz, Acq # 10/10
[11/65]  Freq: 60614010 Hz, Acq # 10/10
[12/65]  Freq: 61273190 Hz, Acq # 10/10
[13/65]  Freq: 62115470 Hz, Acq # 10/10
[14/65]  Freq: 62872310 Hz, Acq # 10/10
[15/65]  Freq: 63470450 Hz, Acq # 10/10
[16/65]  Freq: 64276120 Hz, Acq # 10/10
[17/65]  Freq: 65106200 Hz, Acq # 10/10
[18/65]  Freq: 65850830 Hz, Acq # 10/10
```

ADU 1.0 Test Software

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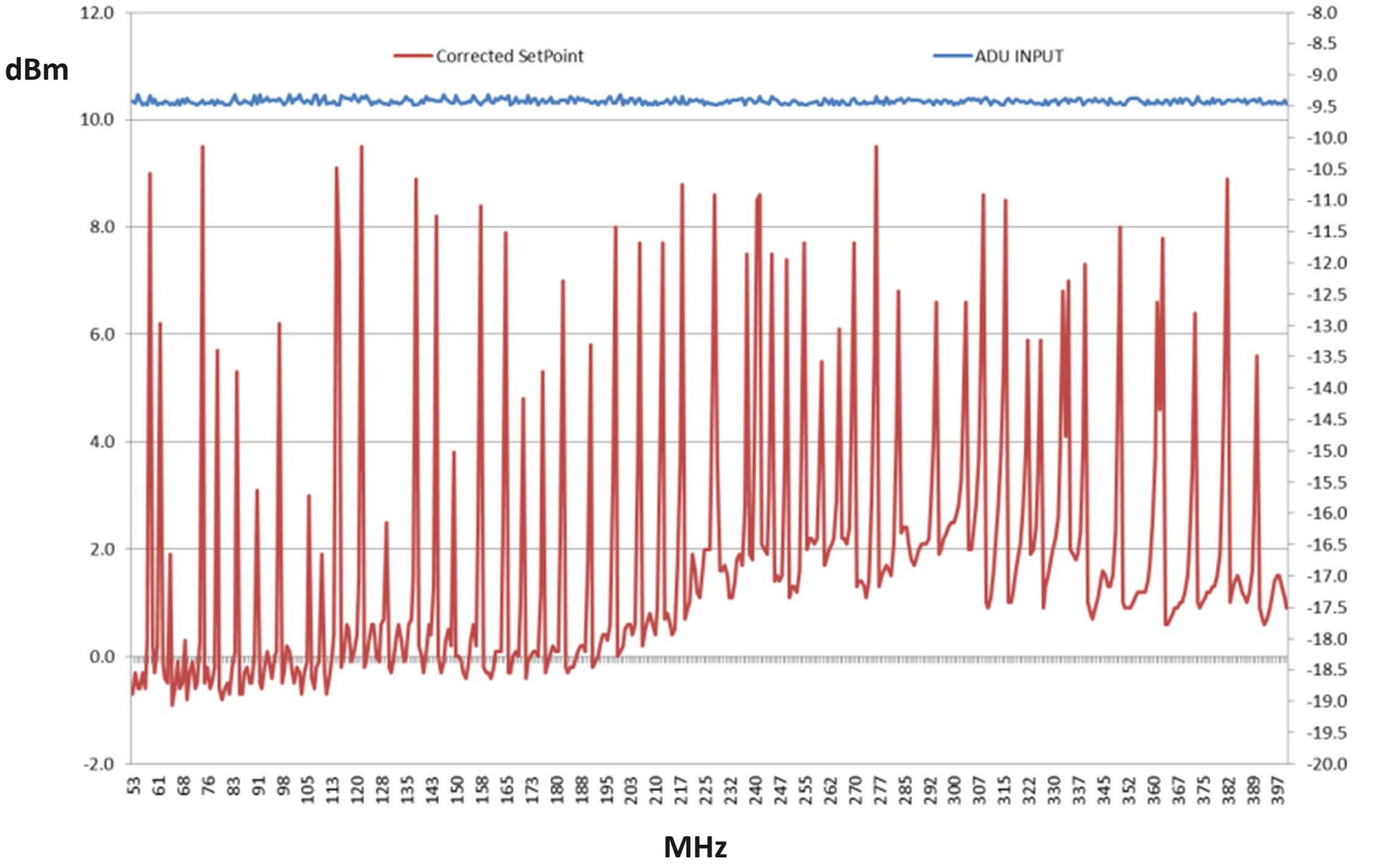


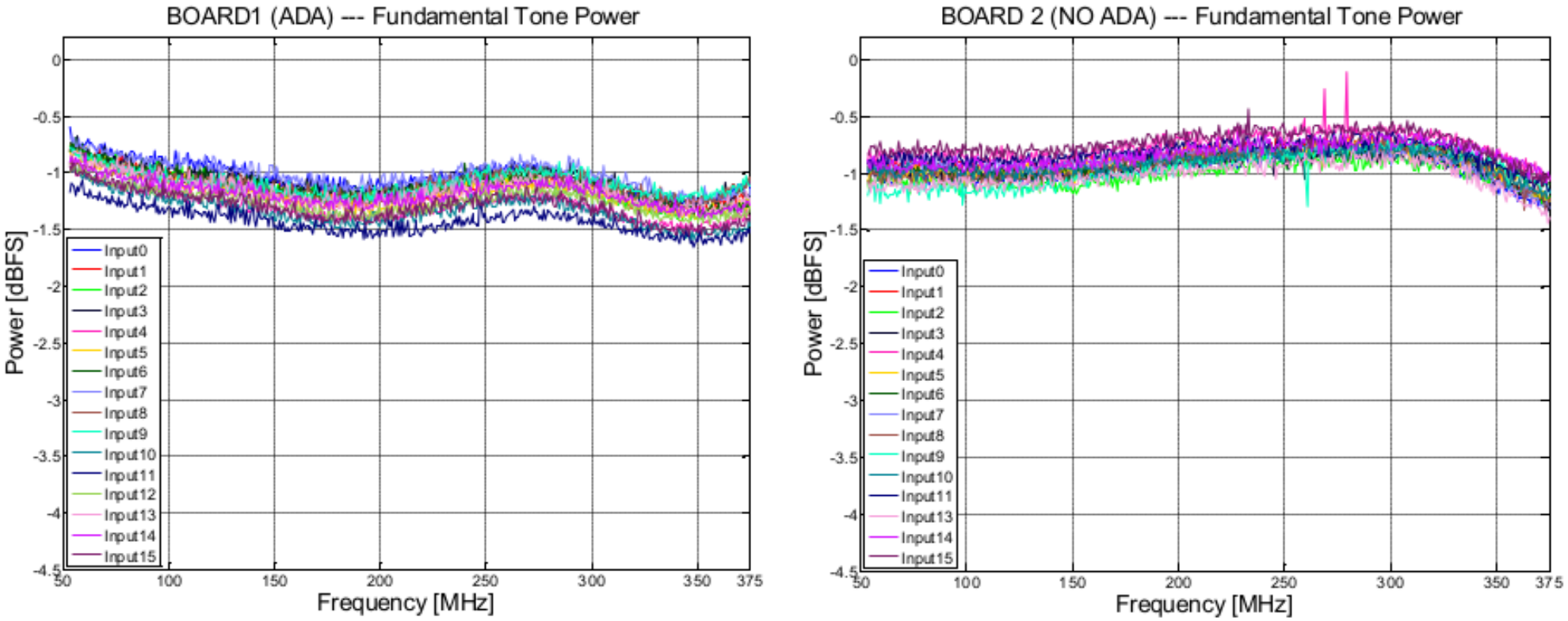


Figure 22: Gain Flatness in Low Frequency Band.

ADU Performance

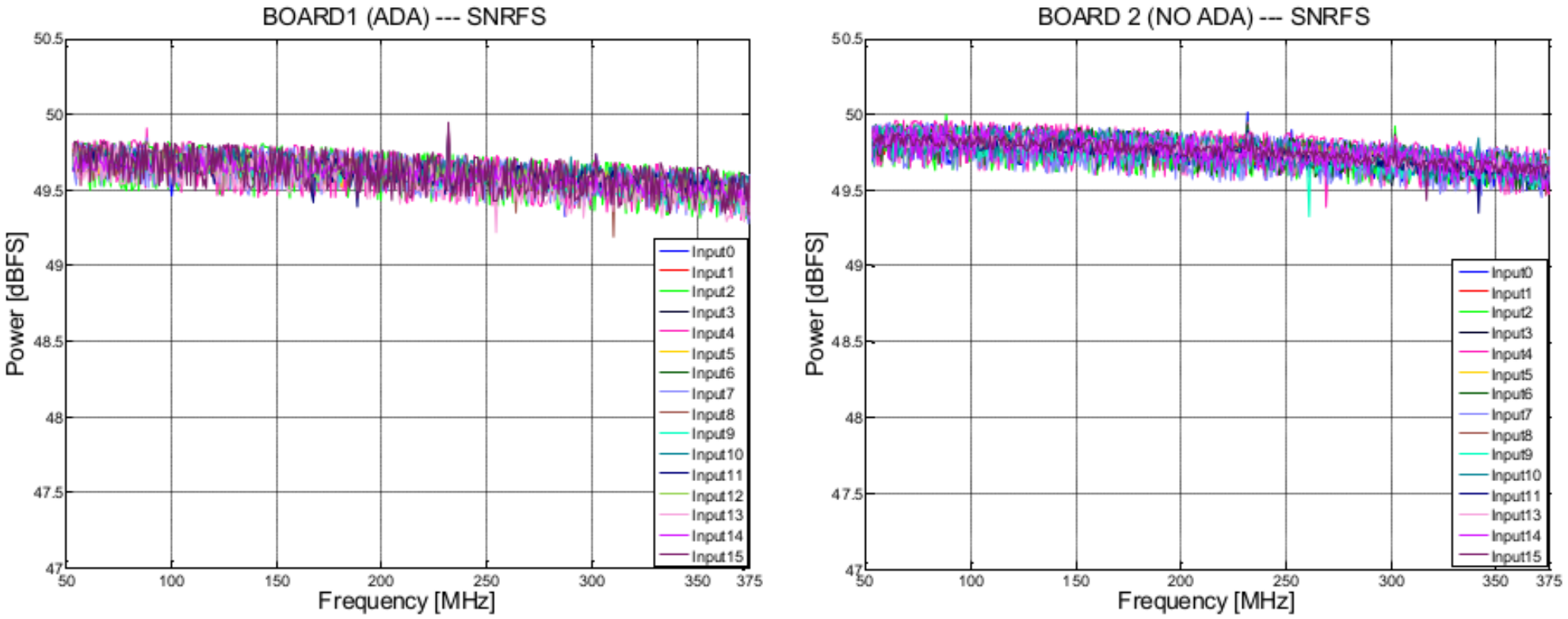


Figure 21: Signal to Noise Ratio referenced to Full Scale (SNRFS) in Low Frequency Band.

ADU Performance

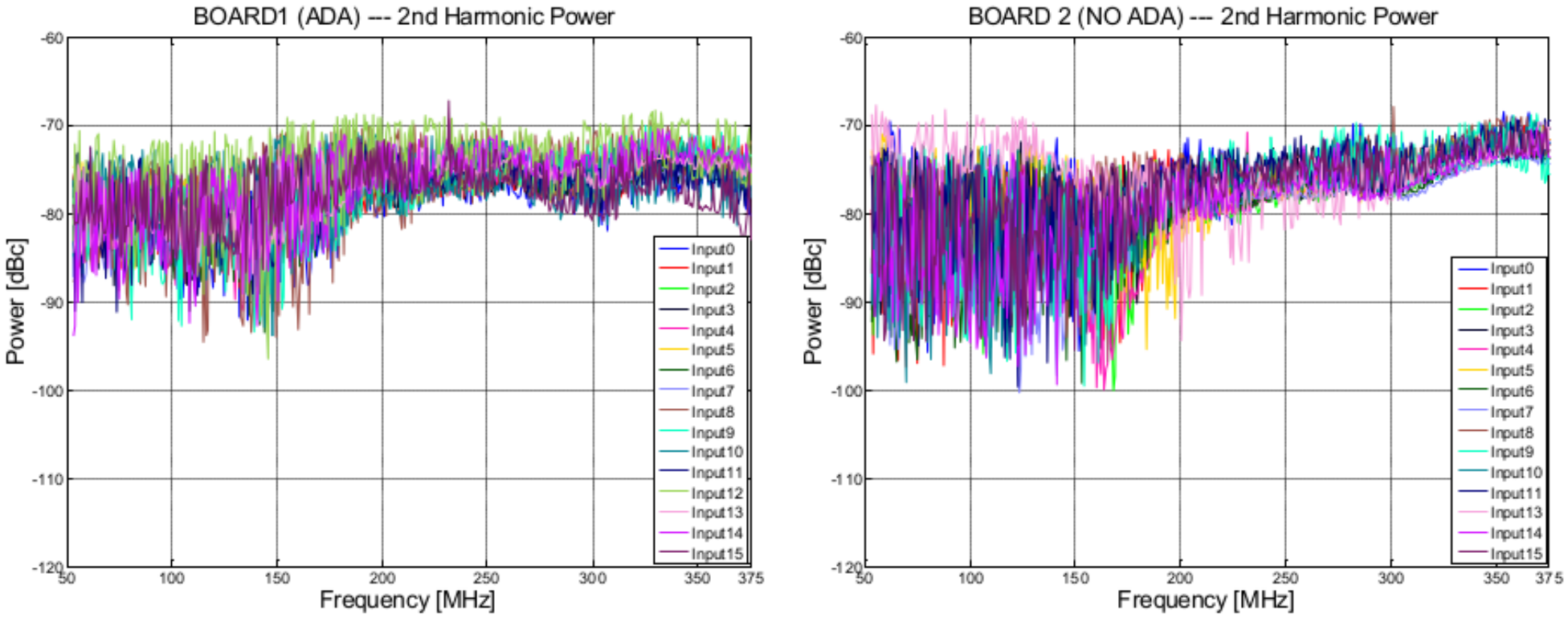


Figure 23: 2nd-order Harmonic Distortion Power in Low Frequency Band.

ADU Performance

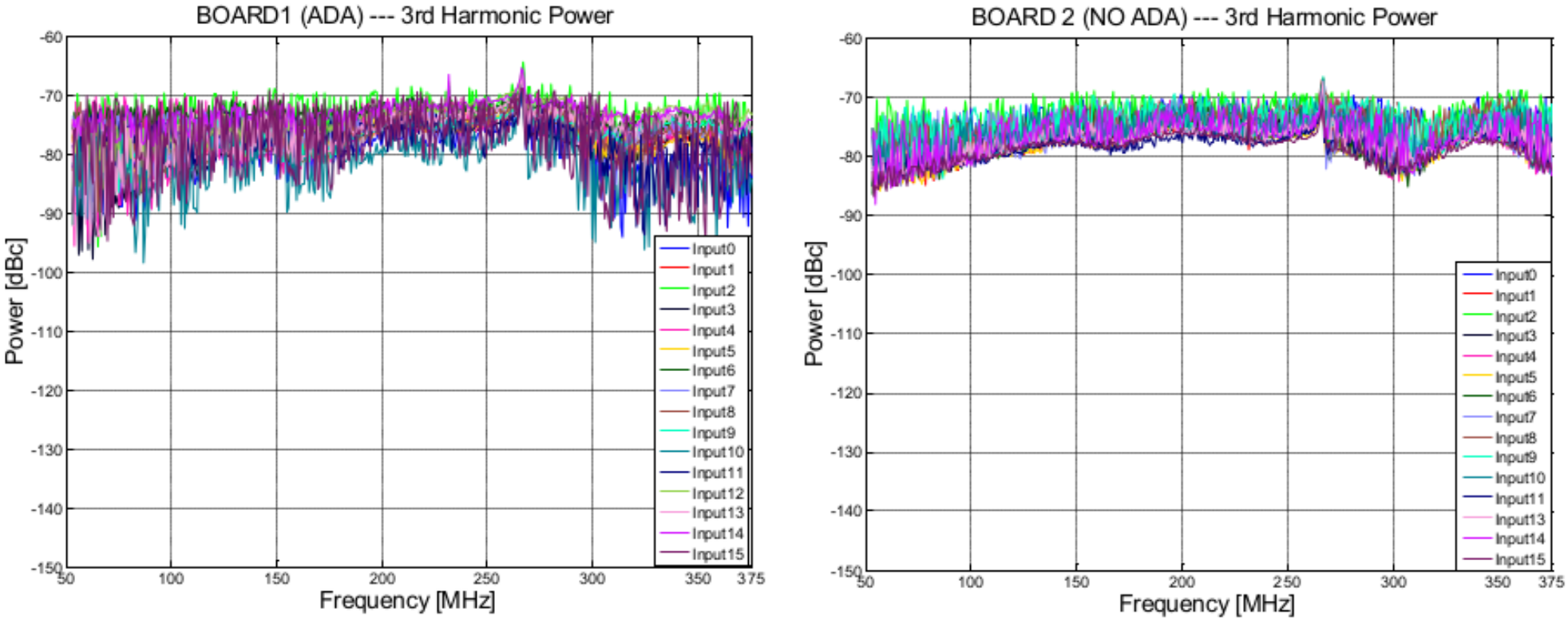


Figure 24: 3rd-order Harmonic Distortion Power in Low Frequency Band.

ADU Performance

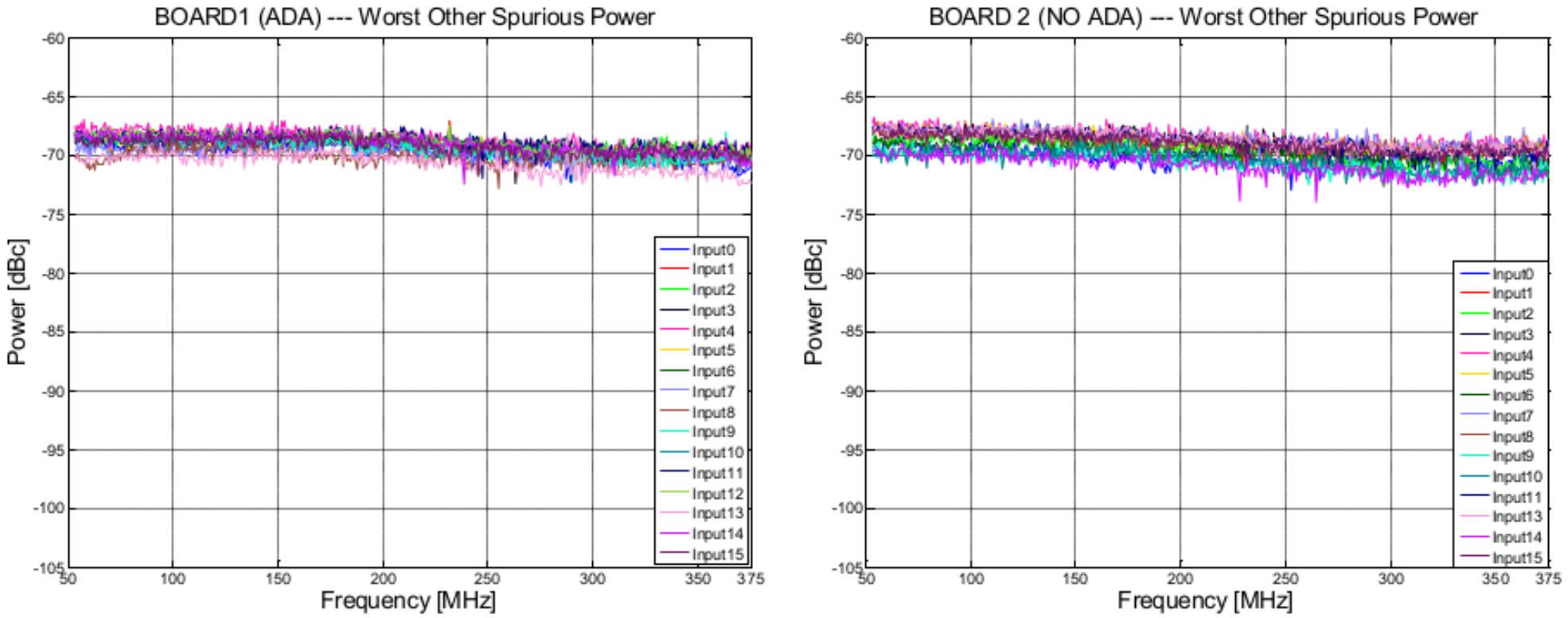


Figure 25: Worst Other Spurious Power in Low Frequency Band.

ADU Performance

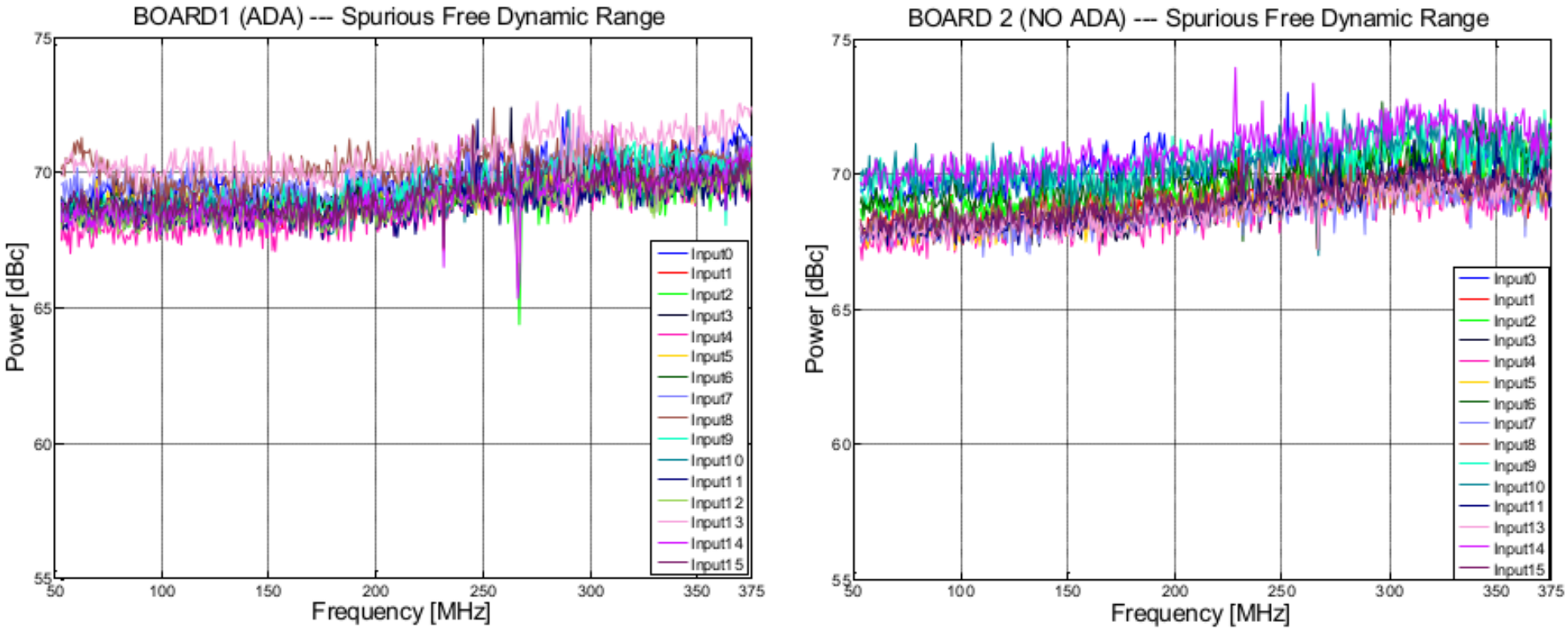


Figure 26: Spurious Free Dynamic Range in Low Frequency Band.

ADU Performance

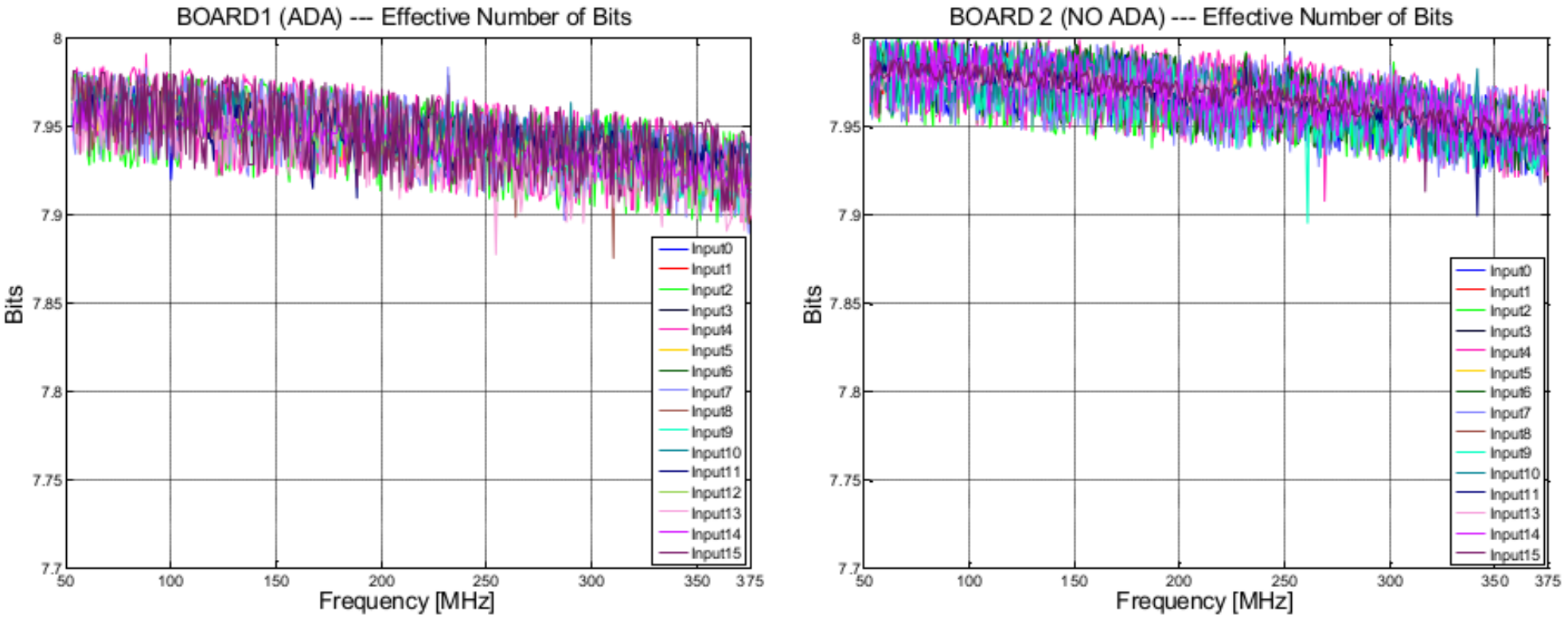
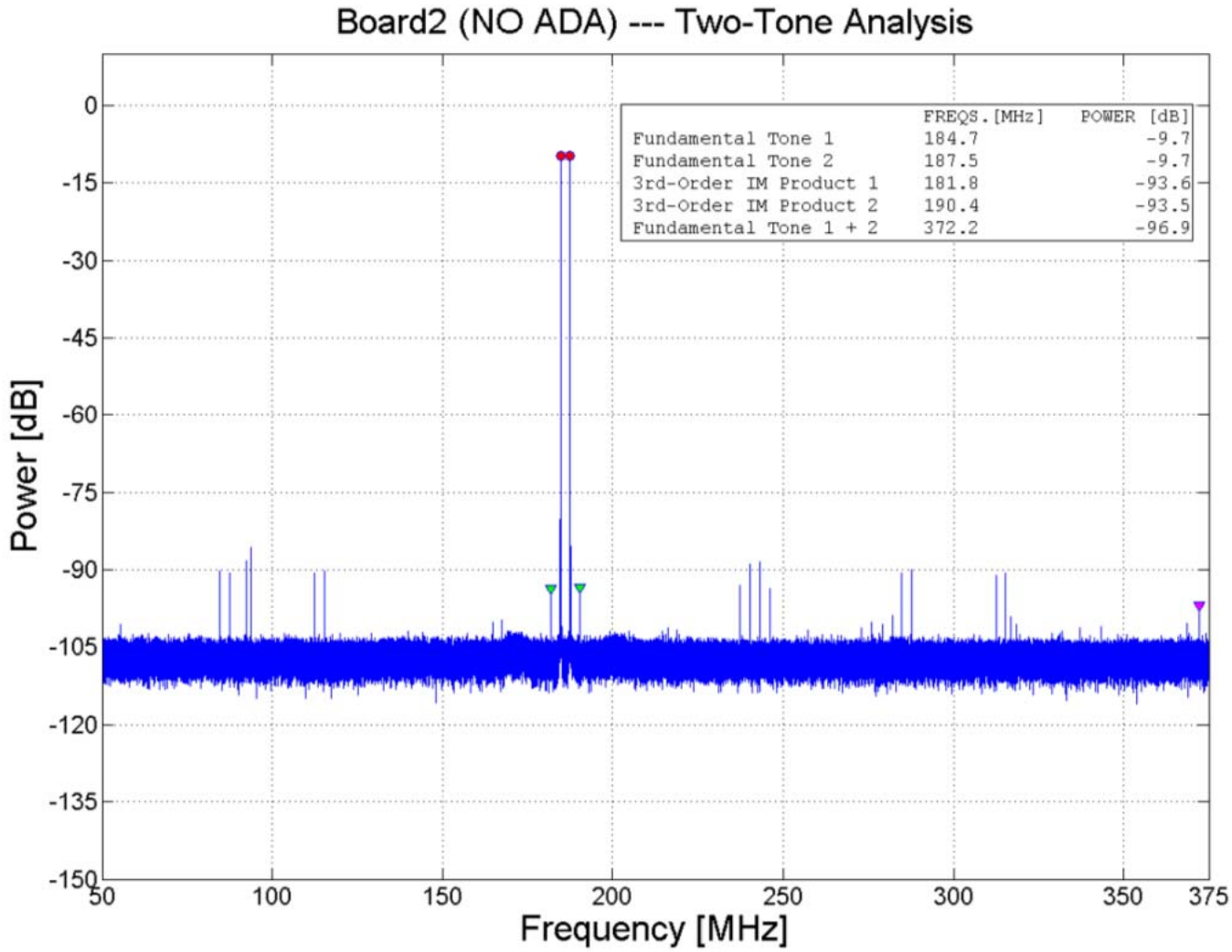
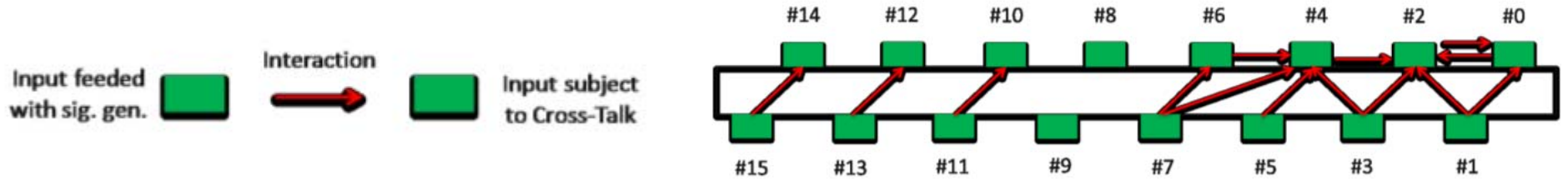


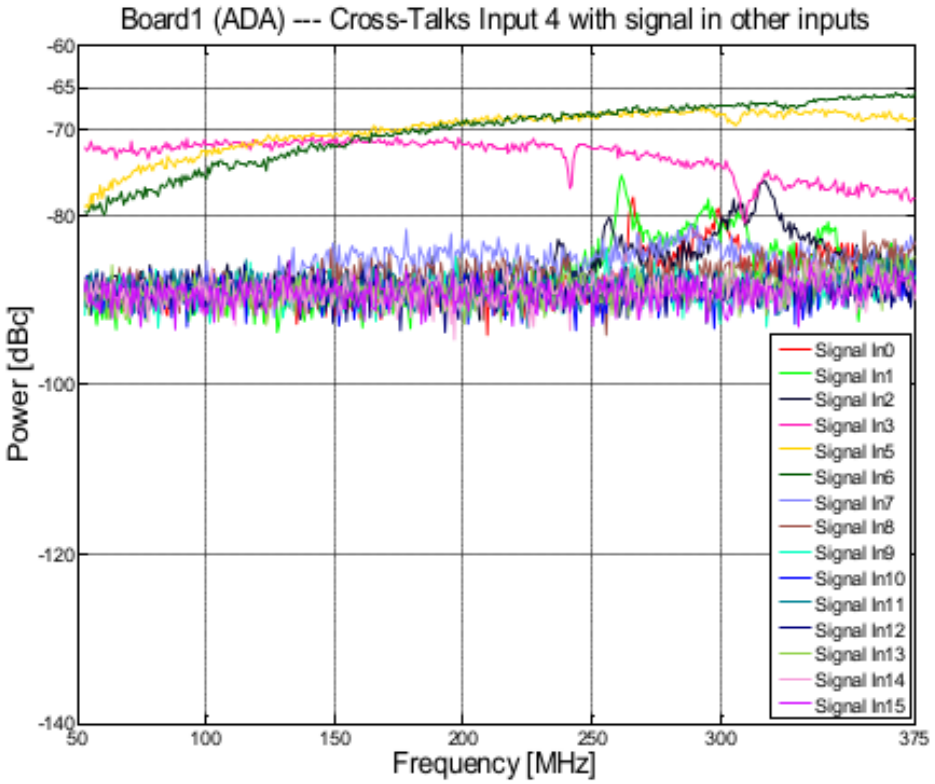
Figure 27: Effective Number of Bits in Low Frequency Band.

ADU Performance



ADU Performance





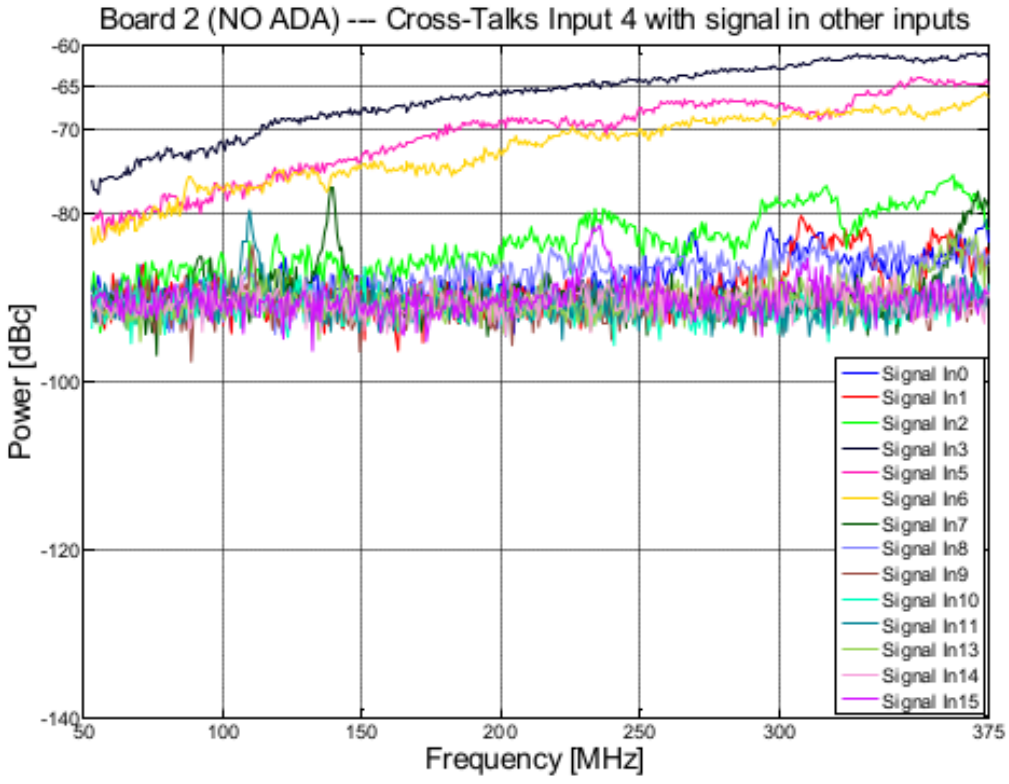


Figure 31: Worst case of Cross-Talk level in Low Frequency Band.

Fs: 800 MSPS --- BW: 50 ÷ 375 MHz		
ADC Performance Parameters	**ADU Board#1 (with ADA)**	**ADU Board#2 (without ADA)**
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 49.19	**≥ 49.33**
Gain Flatness [dBFS]	≤ ±0.3573	**≤ ±0.343**
2nd-order Harmonic Distortion [dBc]	≤ -67.24	**≤ -67.74**
3rd-order Harmonic Distortion [dBc]	≤ -66.53	**≤ -68.56**
Worst Other Spur [dBc]	**≤ -67.03**	≤ -66.83
Spurious Free Dynamic Range [dBc]	≥ 66.53	**≥ 66.83**
ENOB [bits]	≥ 7.876	**≥ 7.896**
Cross-Talk [dBc]	**≤ -65.69**	≤ -61
IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	29.55	**32.2**
IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	66.3	**77.5**

ADU Performance

ADU Test Timing

- Selected 500 “mono spaced” frequencies per freq. range

- Tunable Passband Filter combined with Low Pass and High Pass Filters

- Using VNA for two tone analysis

- 2 Week to test one board (2 frequency range)

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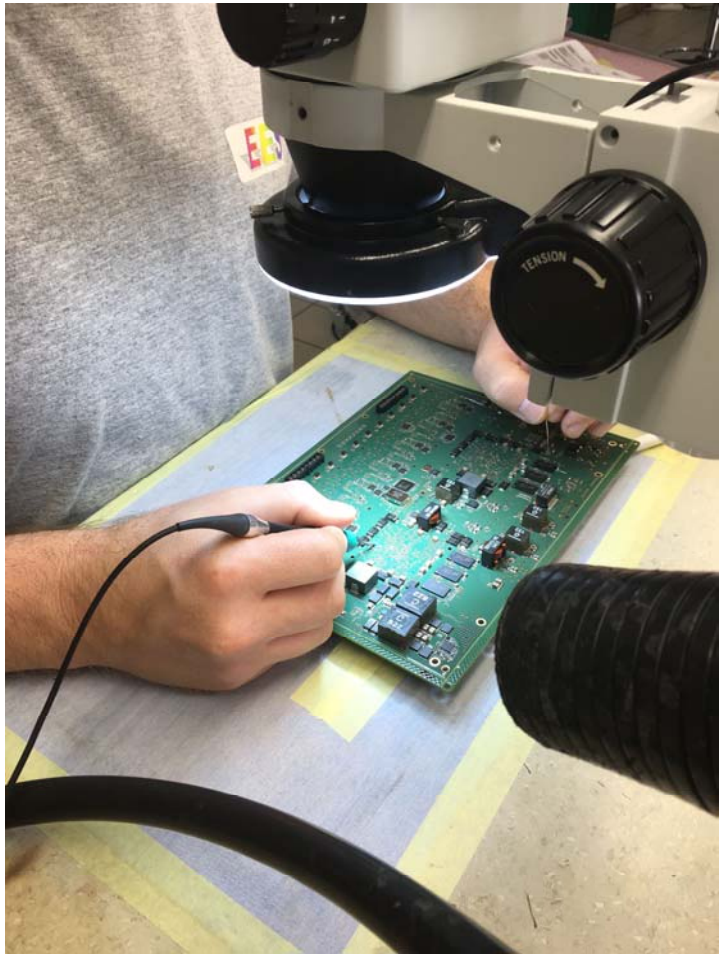

AAVS1 Production: 25 ADU, 50 PRE-ADU, 400 RX (+ Spares)

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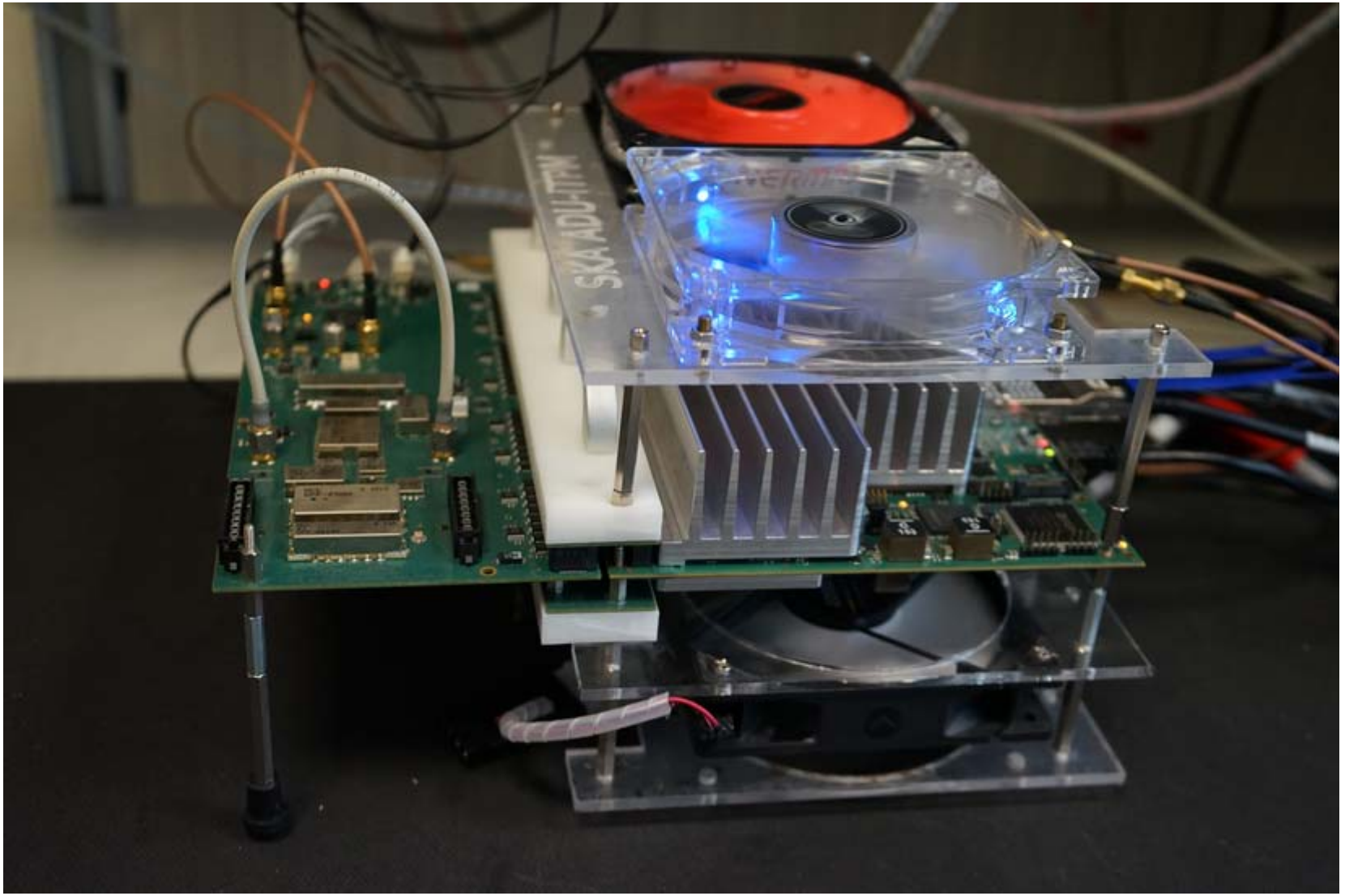

RF JIG

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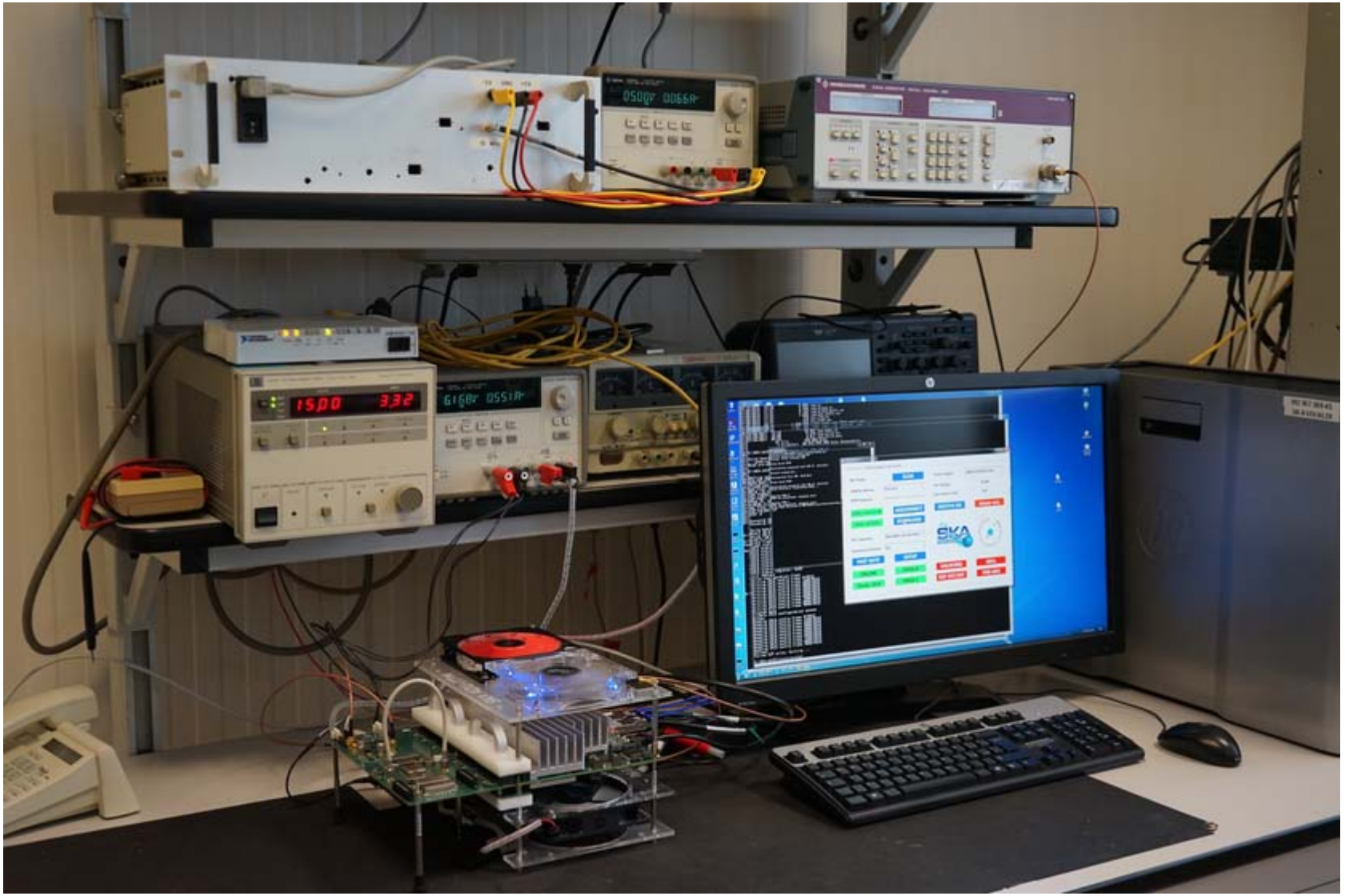

Upgraded Test Setup

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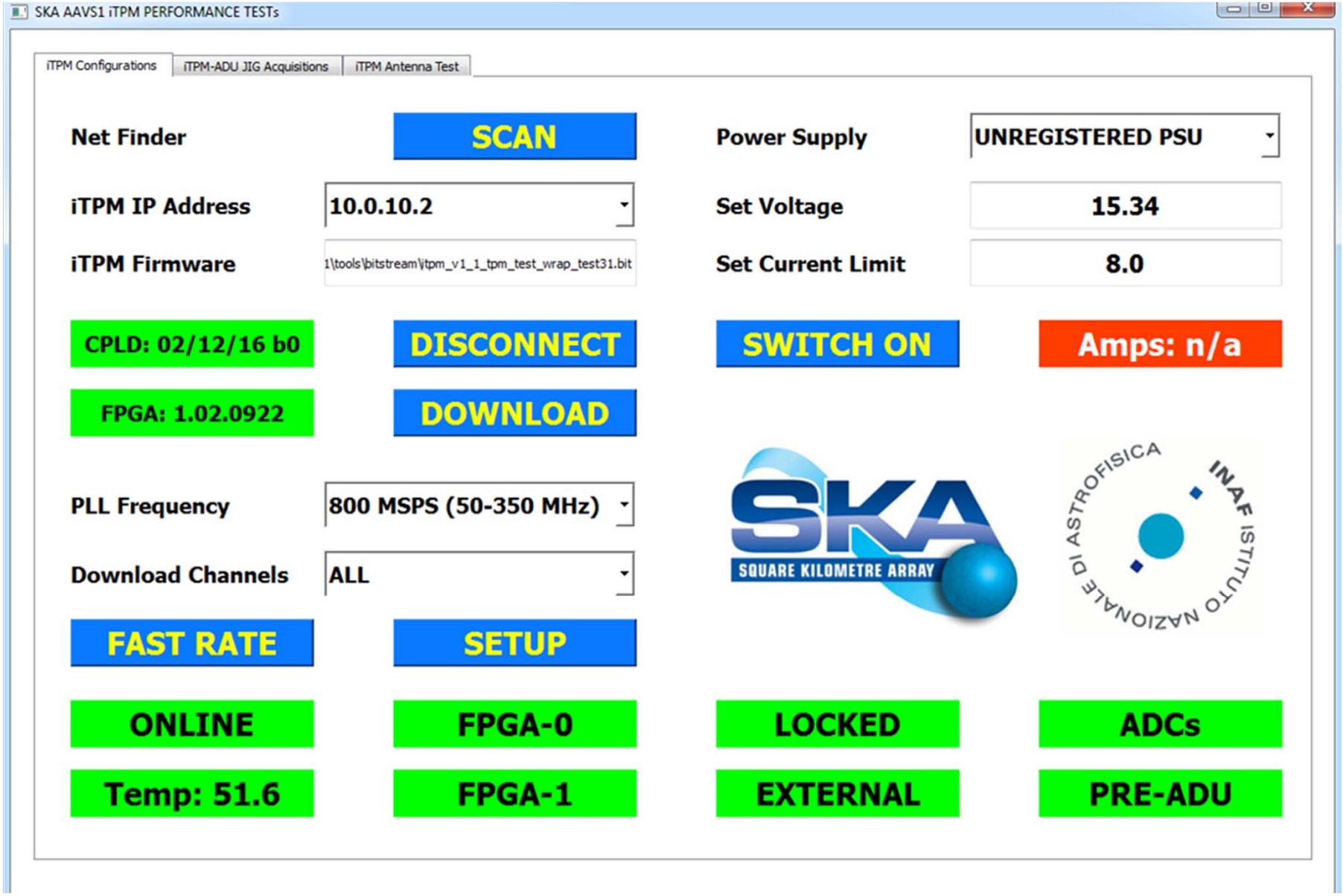

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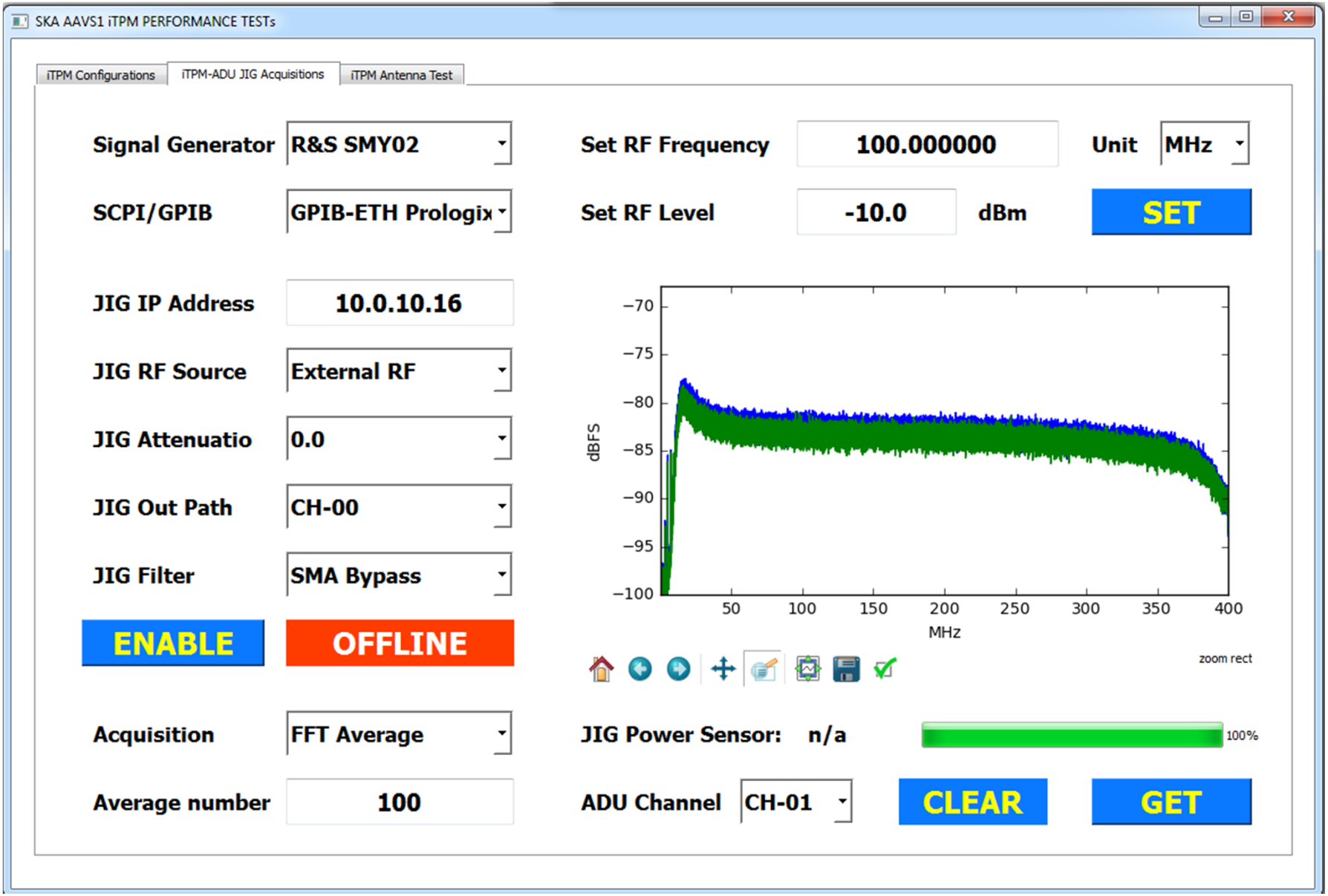

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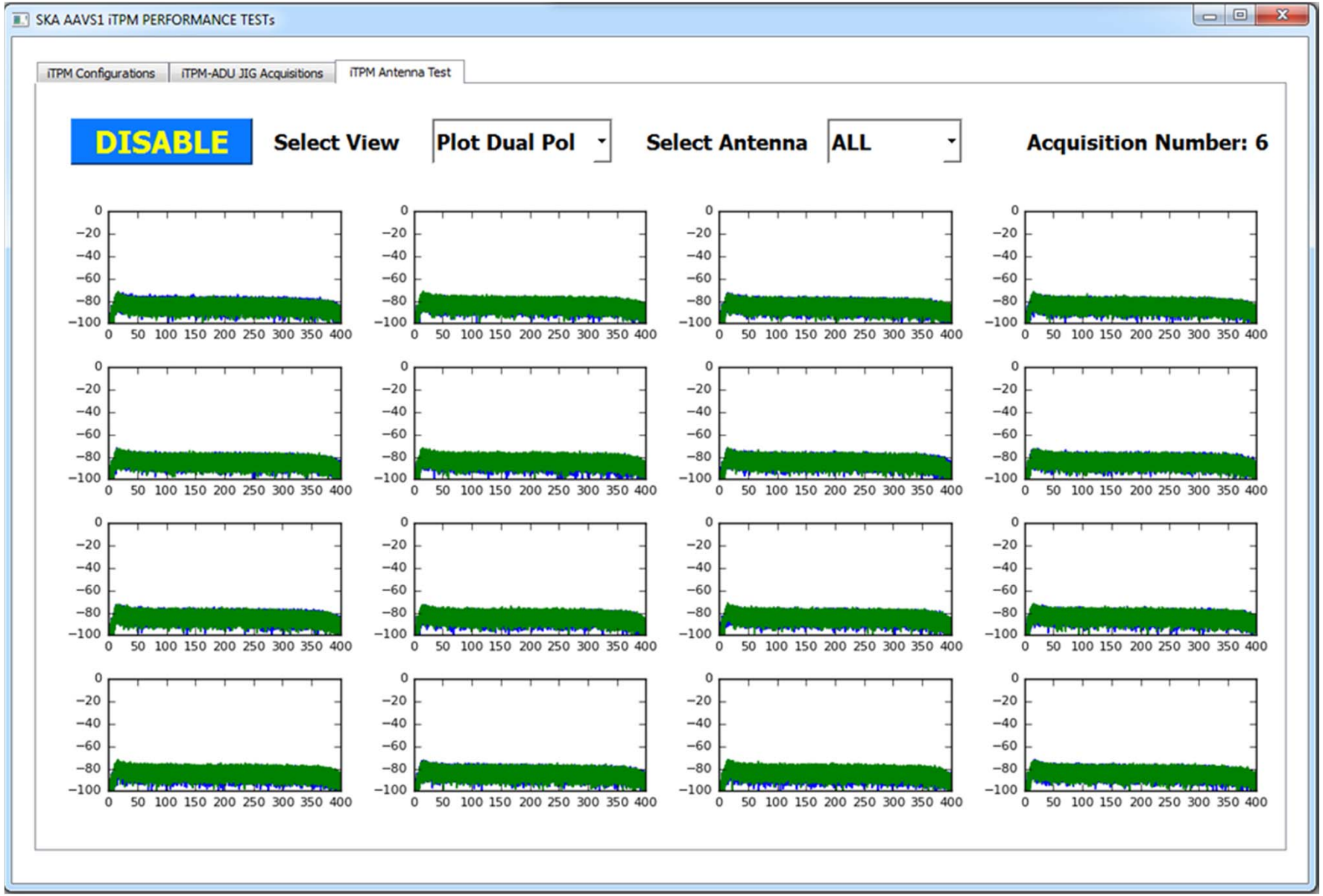

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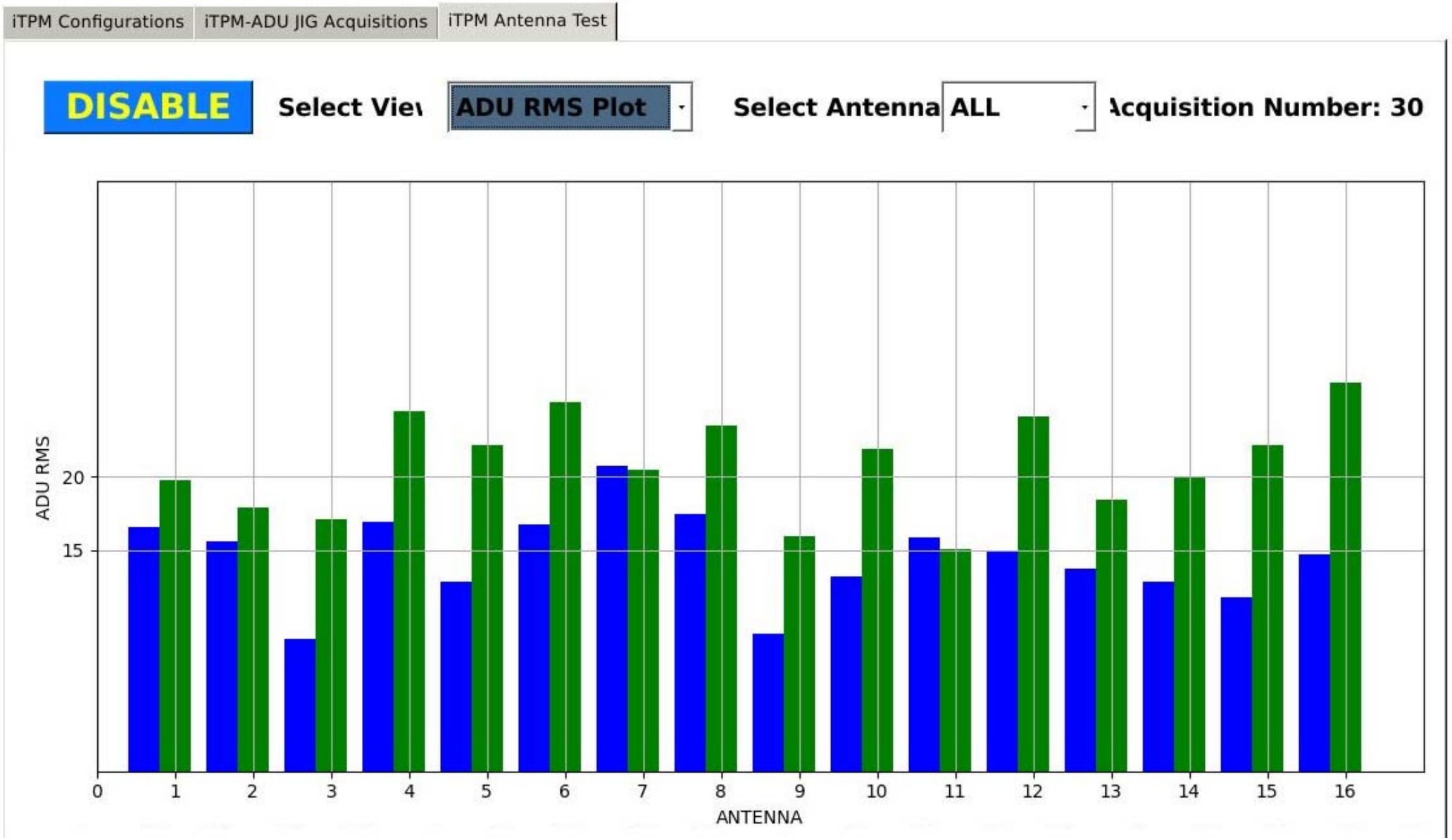

ADU Test Timing

- Selected 500 “mono spaced” frequencies per freq. range

- Tunable Passband Filter combined with Low Pass and High Pass Filters

- Using VNA for two tone analysis

- 2 Week to test one board (2 frequency range)

- Selected 20 “mono spaced” frequencies

- Fully Automated test bench

- 20 Minutes per frequency range

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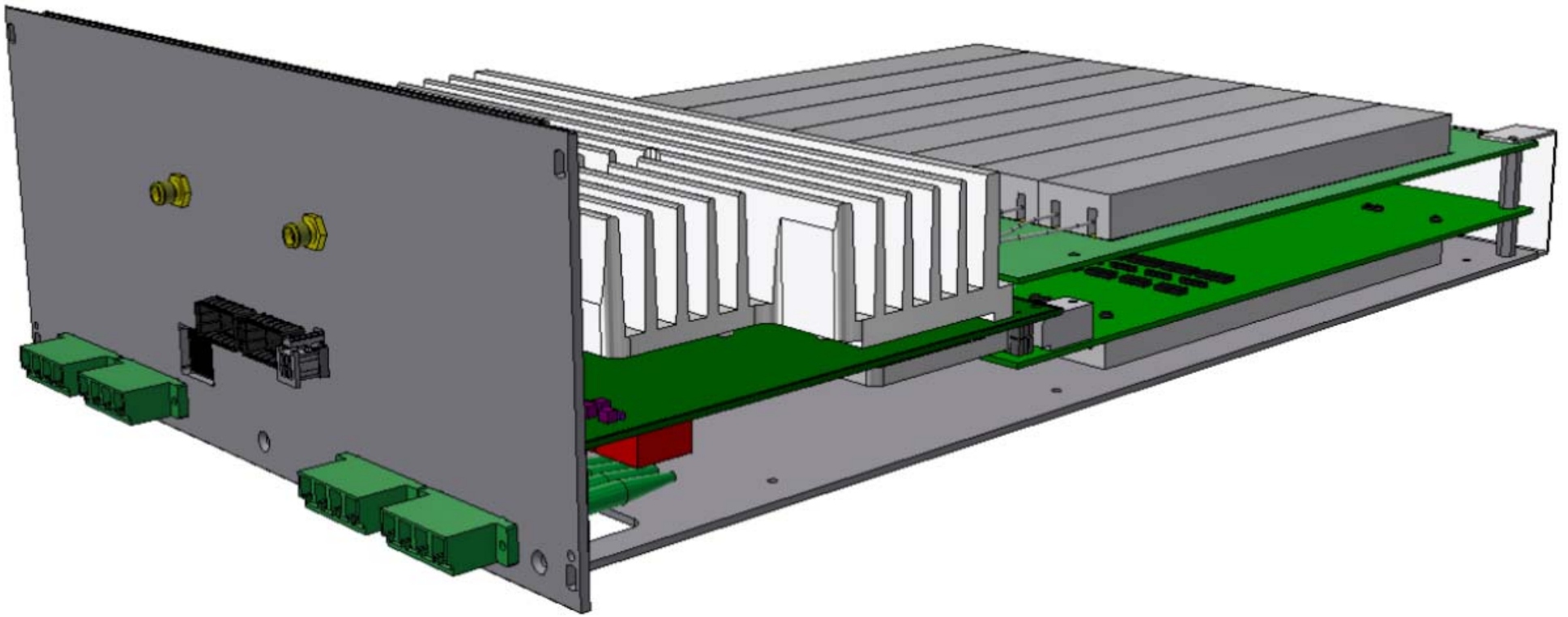

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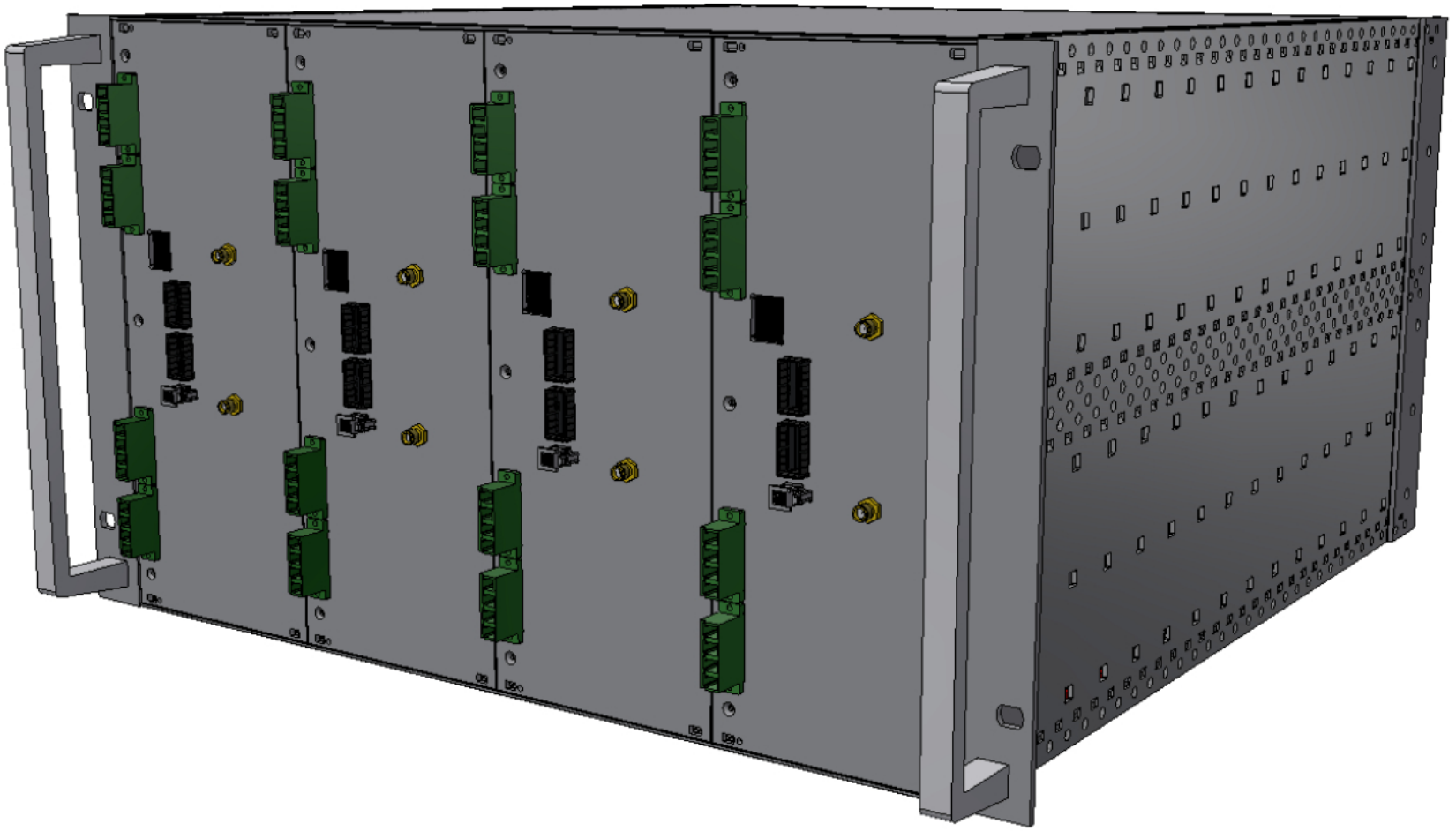

iTPM Subrack

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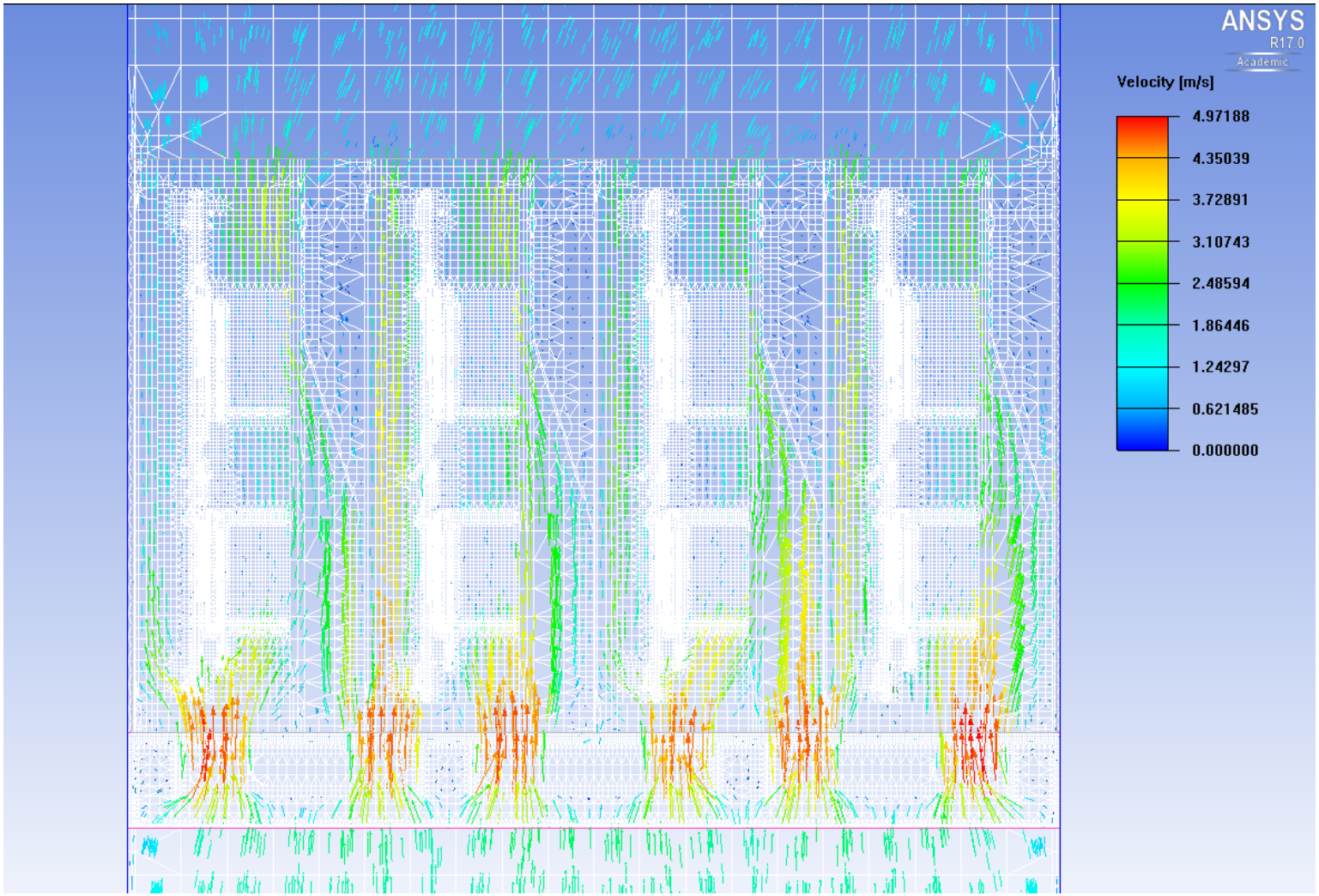

SubRack Thermal Analysys

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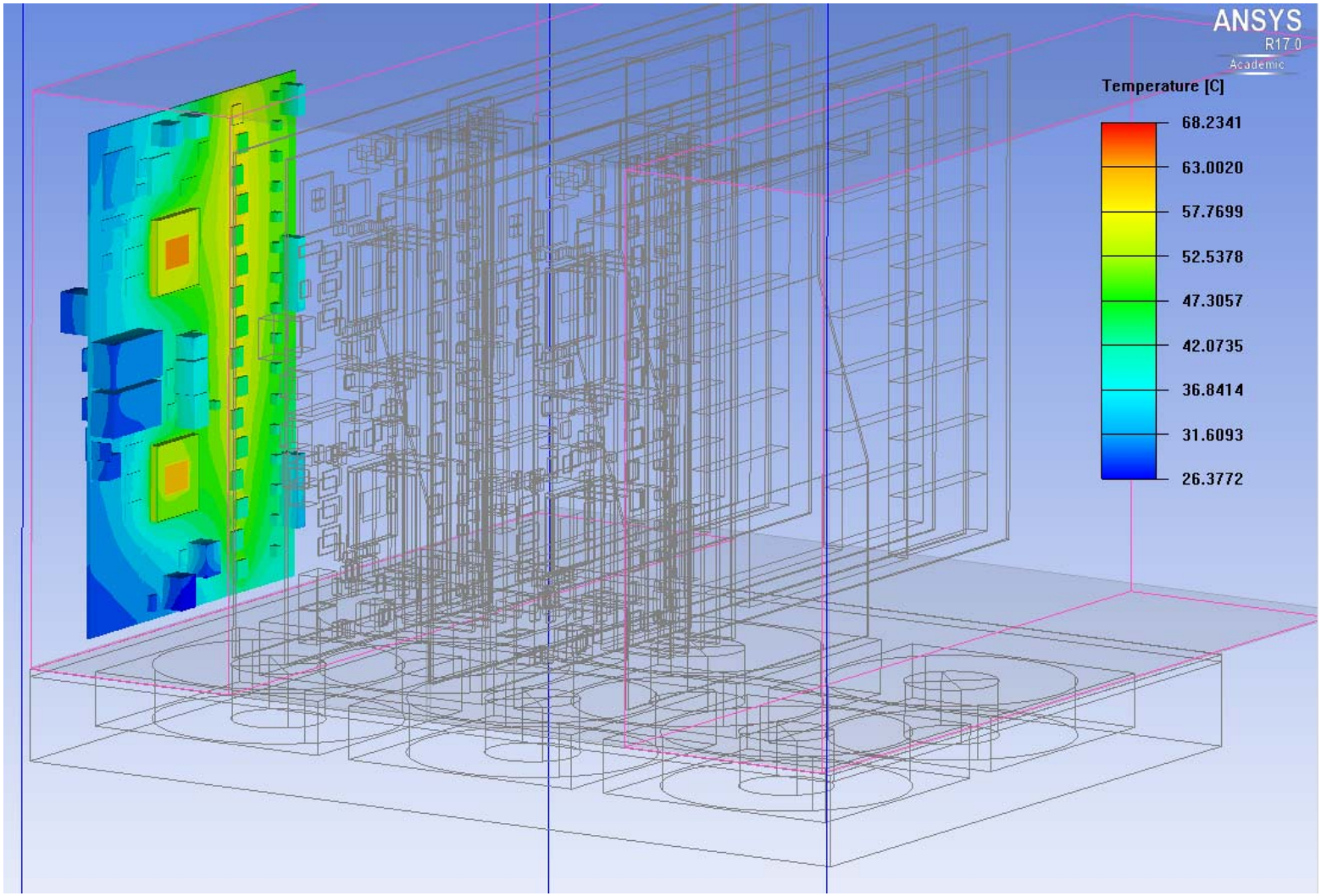

SubRack Thermal Analysys

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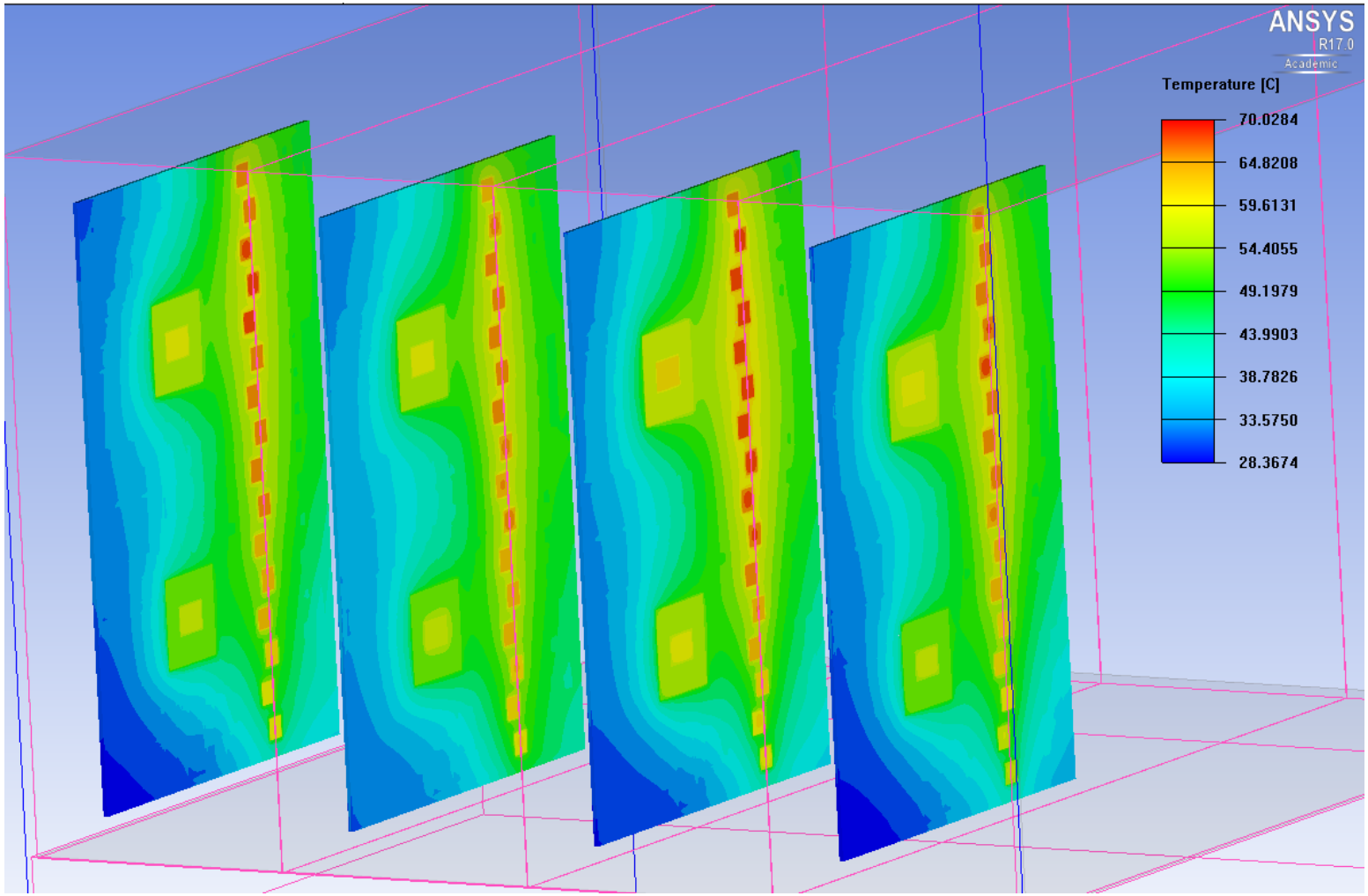

SubRack Thermal Analysys

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SKA AAVS1 main station
deployed on November 2017

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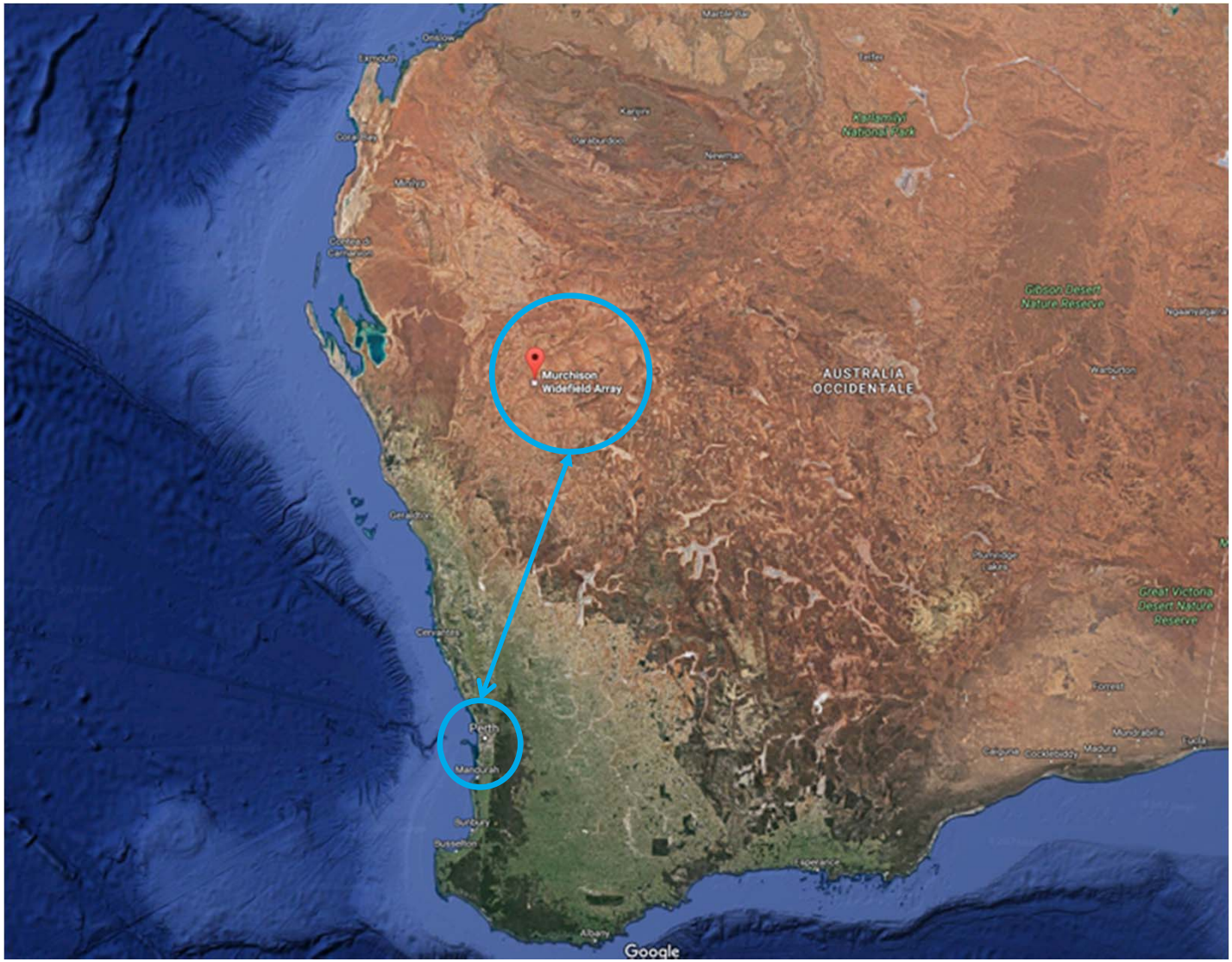

SKA AAVS1 Murchison Western Australia

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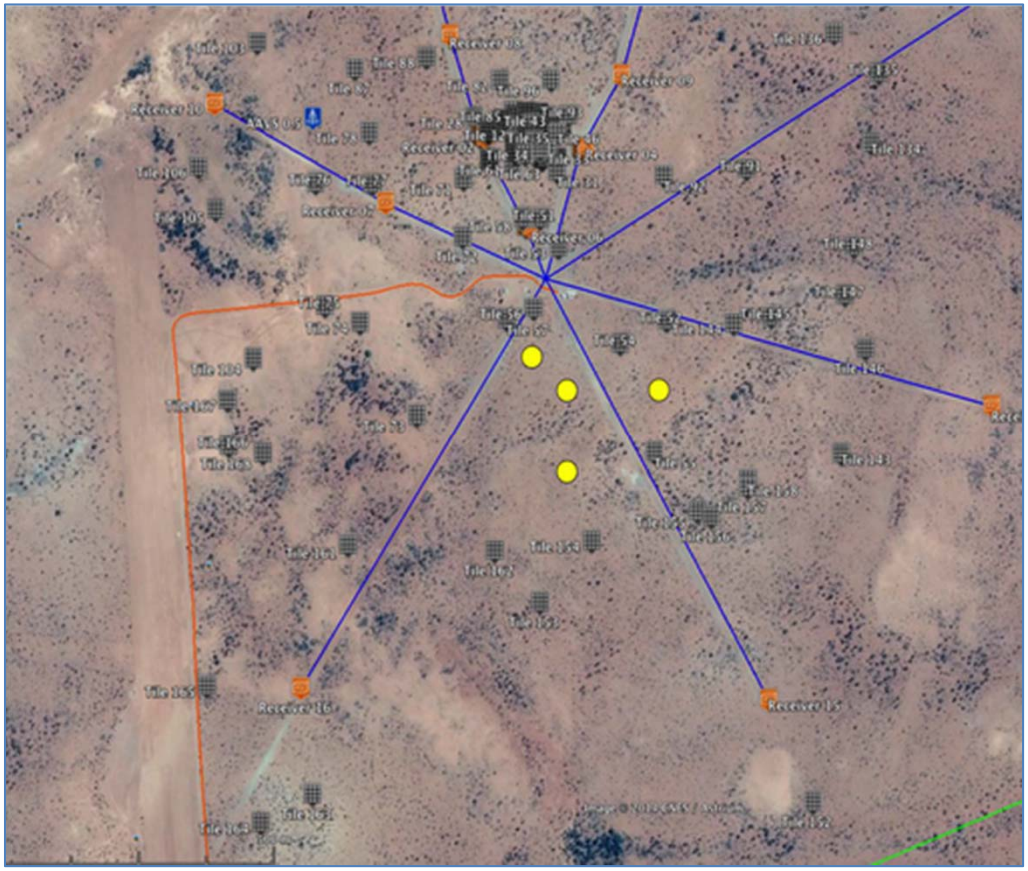

SKA AAVS1 Hosted by MWA Correlator site and Facilities

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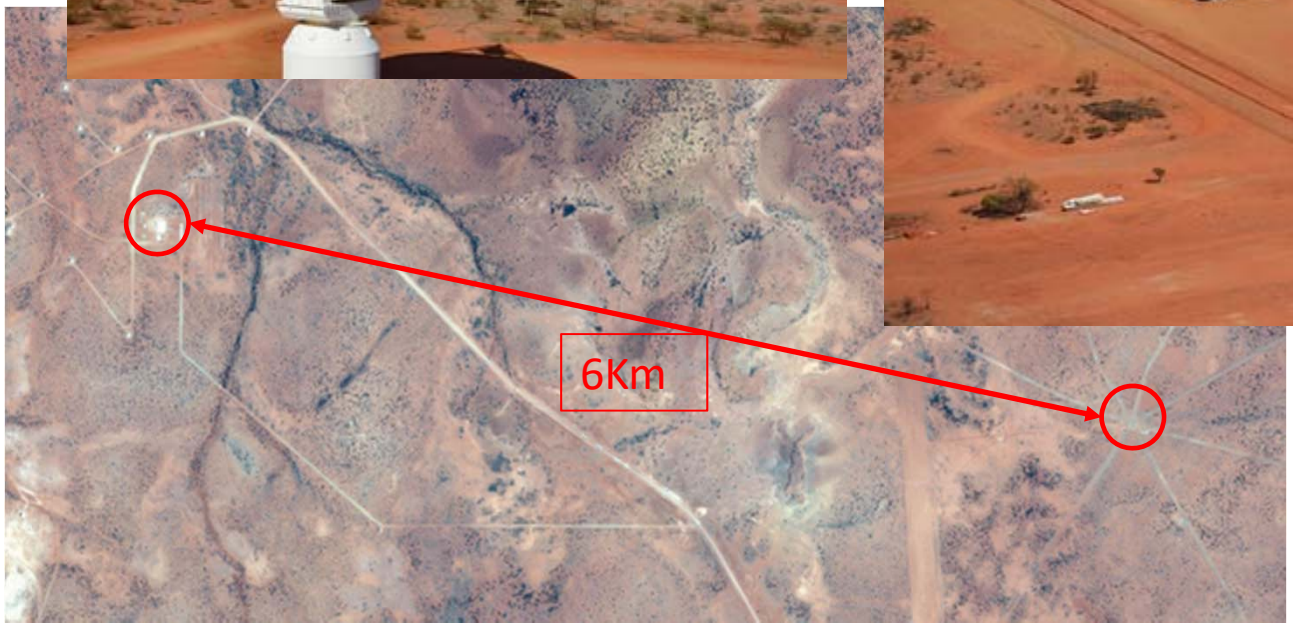

SKA AAVS1 Hosted by MWA Correlator site and Facilities

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AAVS1 ASKAP Control Room (MWA Racks)

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AAVS1 Crew

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AAVS1 Cable Management

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SKA AAVS1 TPM Racks Management

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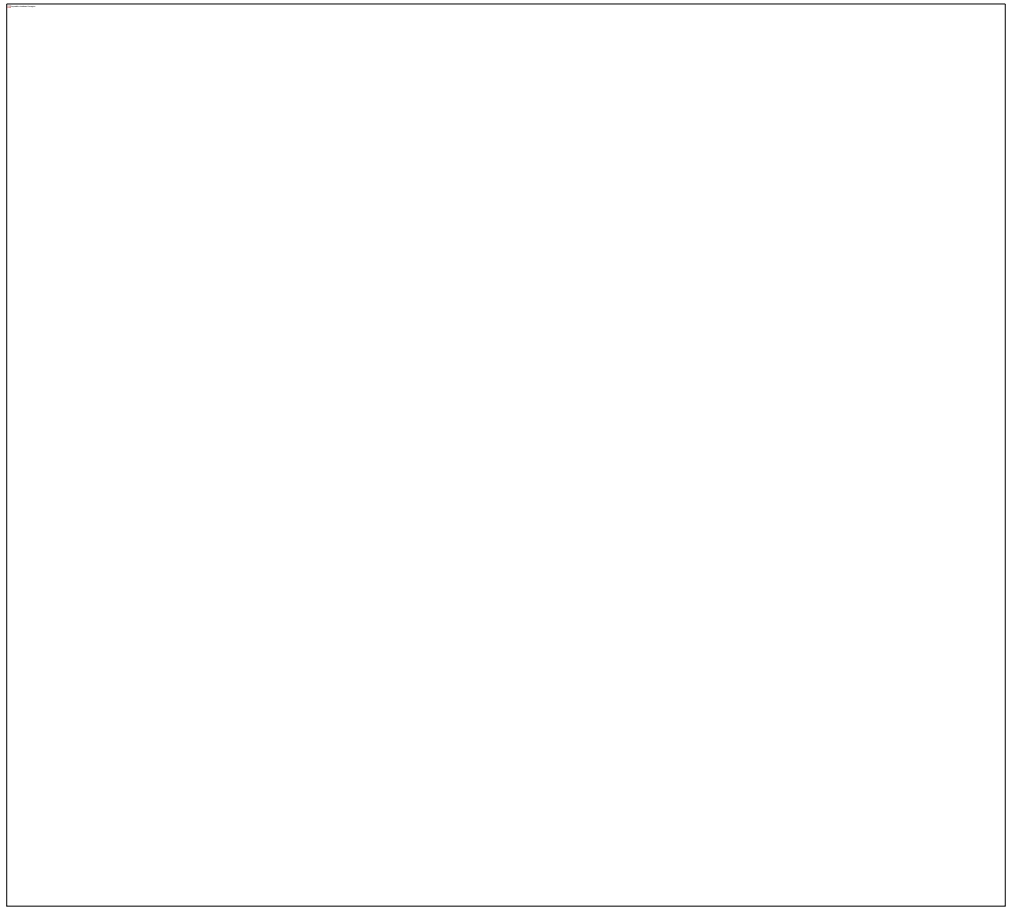
Pol X



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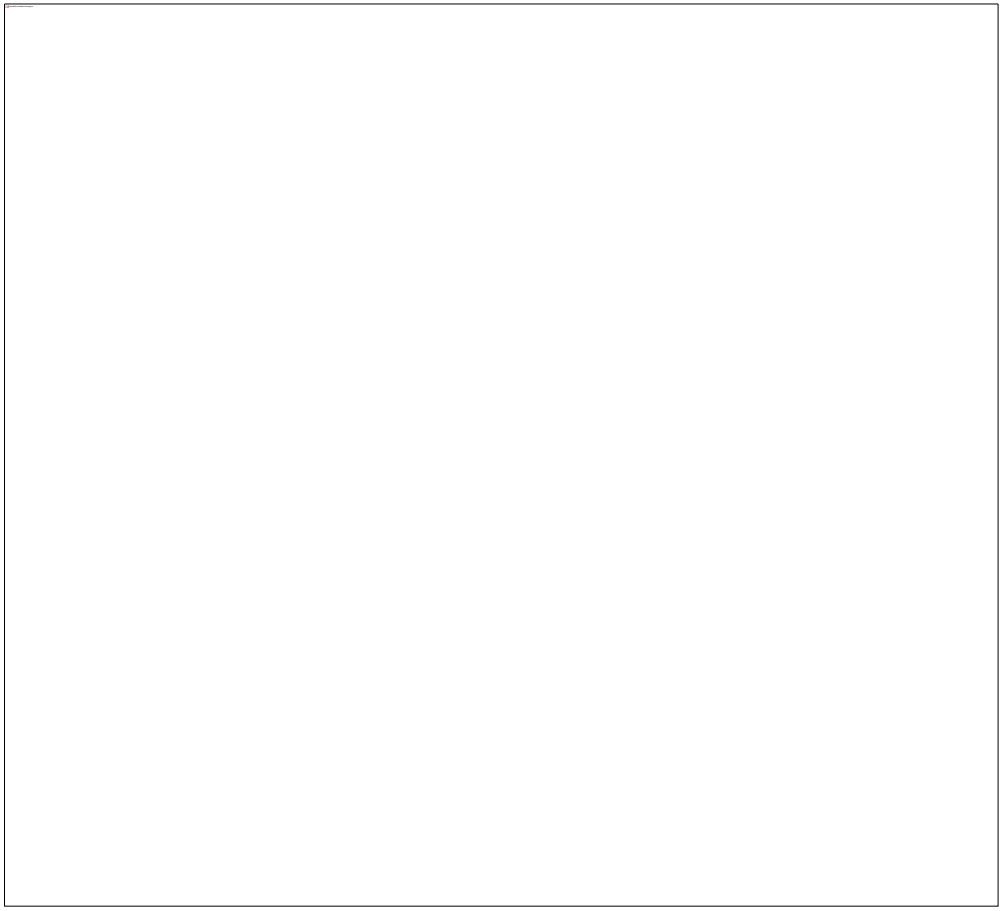

SKA AAVS1 Station Test Software

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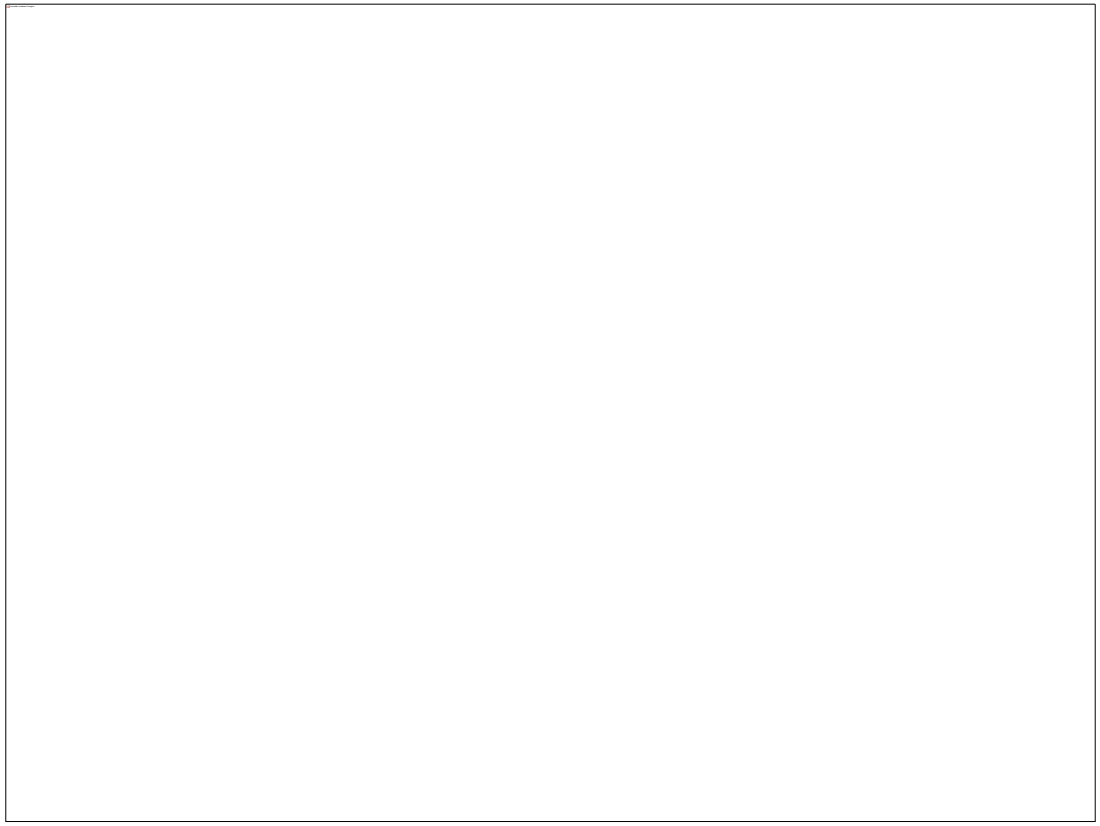

RARE Tropospheric phenomena ever seen ducting RFI around MRO

FM Radio Channels from where???

Current status and future plan

- Logging every day the station using test firmware
- iTPM Station Beamformer FW ready by the end of 2017
- Complete AAVS1 with 3 satellites
- UAV AAVS1 Station Measurements
- iTPM v1.2 boards provided also to SKA-MID
- iTPM v2.0 design still ongoing (8 iTPMs per Subrack including backplane)
- iTPM v1.2 connected to one “EDA” MWA station (16 Beamformed Tiles)
- SAD (128 antennas) to be completed next year
- Medicina BIRALES upgrade to iTPM
- PHAROS 2 iTPM for Phased Array Filter

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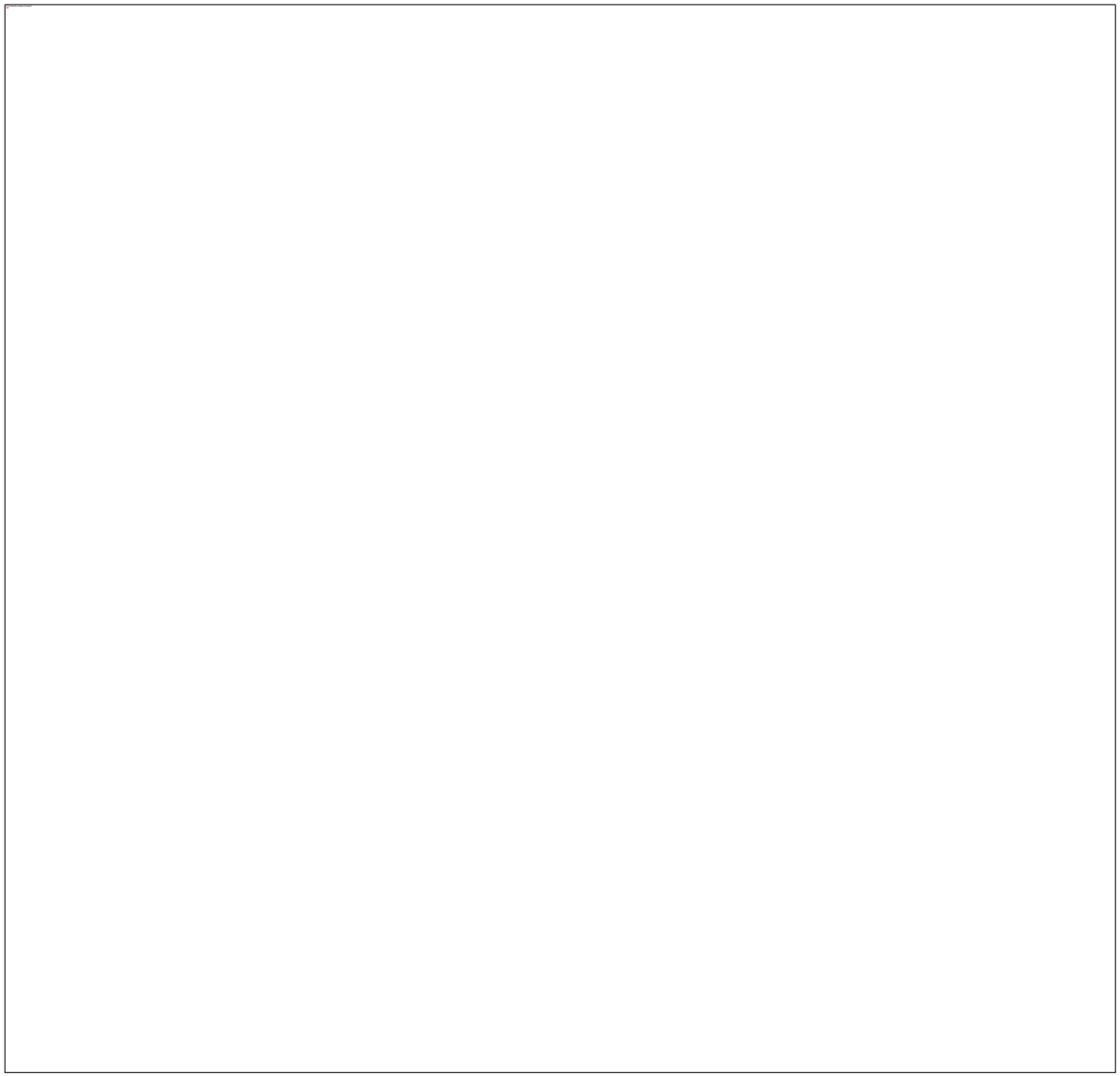

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