R&D Experiences on FPGAs at IASF Milano + astronomical applications

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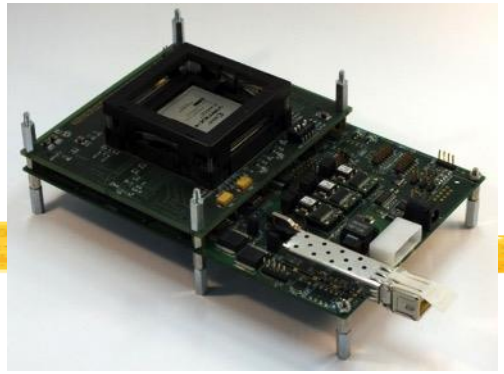
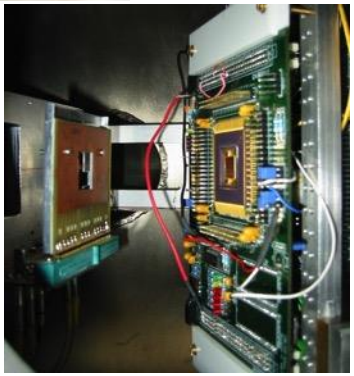
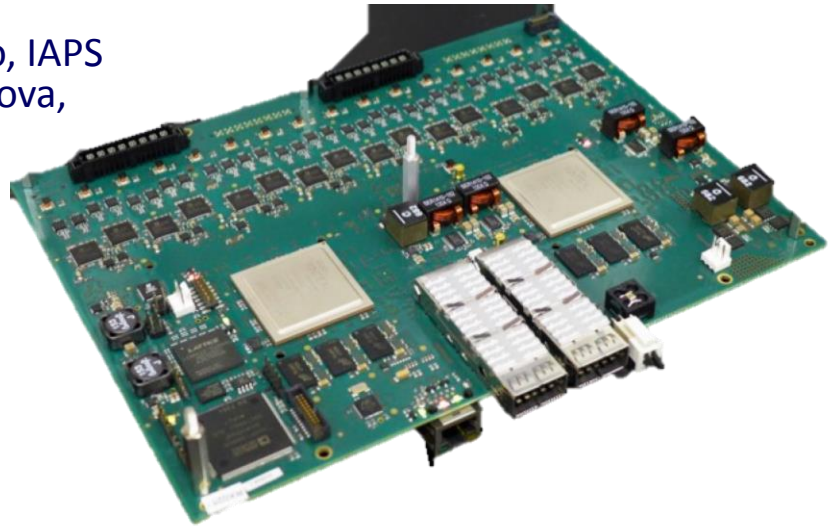
Who we are



- 4 Staff, 4 Research Associates
- Activities
  - Detectors & Front-End Electronics
  - Reliable computing systems
  - Radiation effects of electronics devices
  - Fault tolerance and detection methods for reliable systems



- Collaborations
  - IRA/ORA, OACT, Oss. Arcetri, IASF BO, OATo, IAPS
  - Universities (Milano, Bologna, Firenze, Padova, PoliTO, PoliMI)
  - MPS
  - ESA
  - SANITAS EG
  - OHB/CGS
  - THALES ALENIA SPACE ITALIA

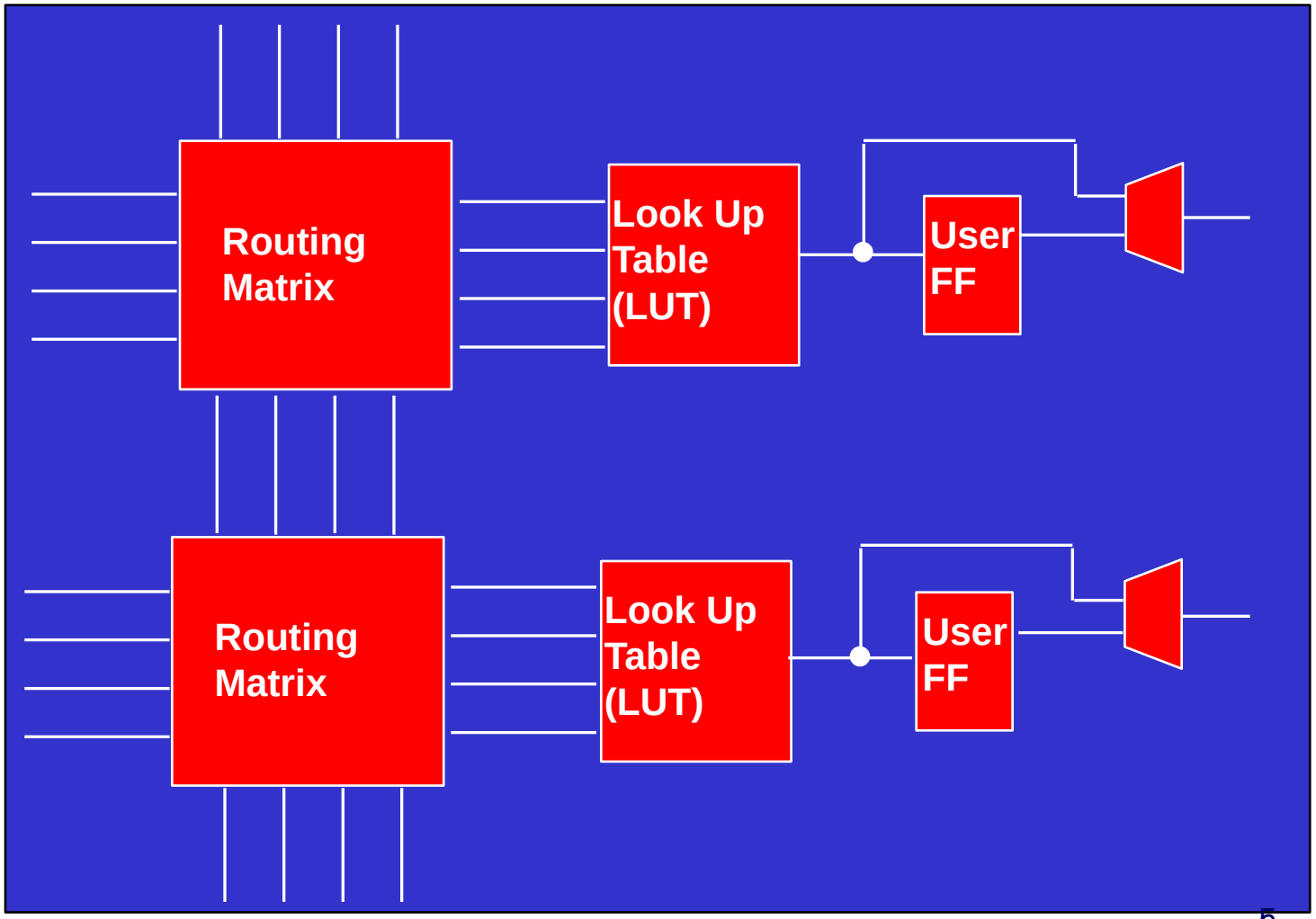


FLIPPER

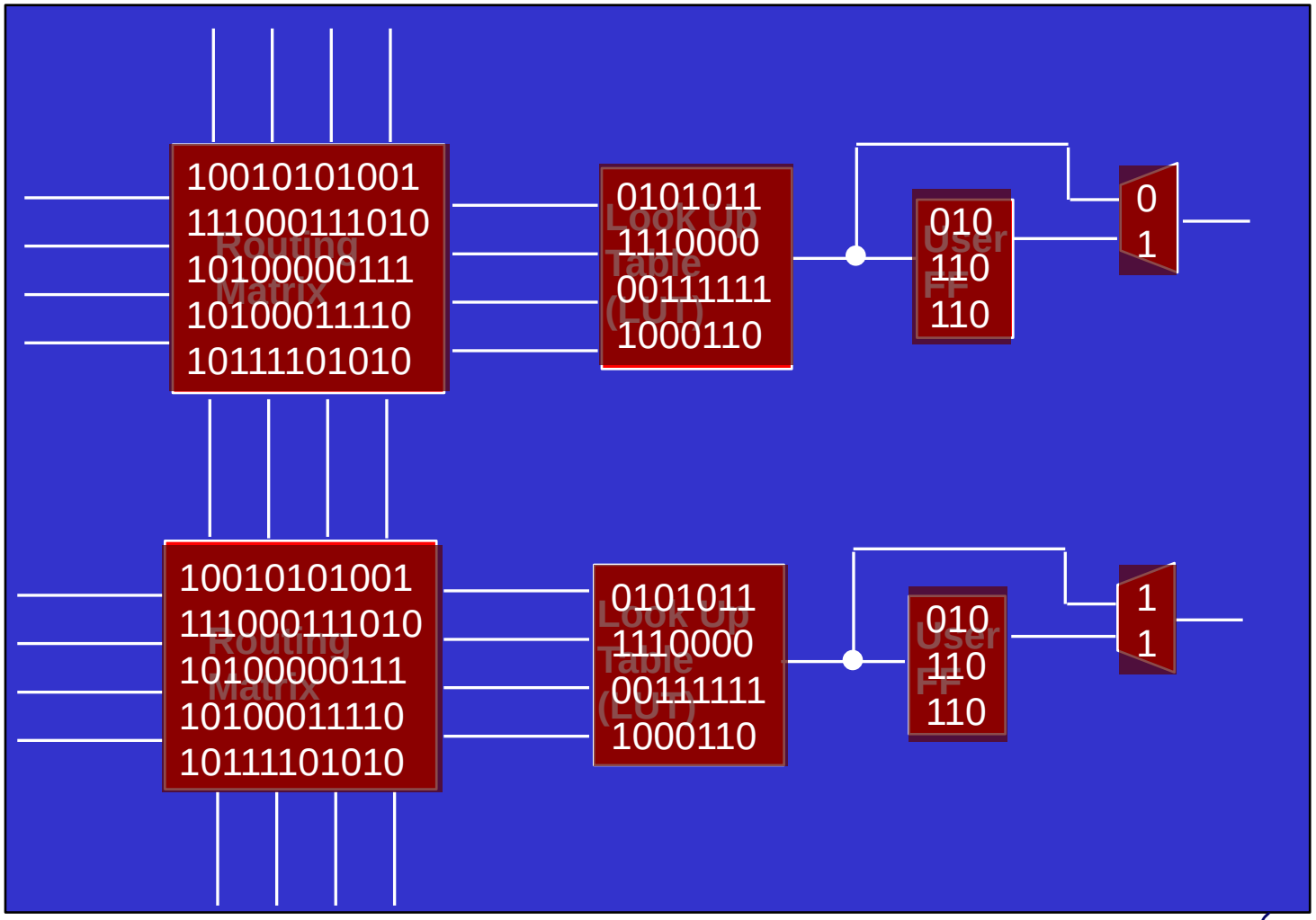
Introducing SRAM-FPGAs……

- ✓Performance
  - ●Can be faster and more efficient than a “standard” processor
  - ●Provide a high density logic (over 1 million gates)
- ✓Flexibility
  - ●FPGA resources can be used for multiple instruments and missions
  - ●Errors in an FGA design can be repaired in orbit
- ✗Single Event Upset (SEU) sensitivity from Heavy Ions and Protons
- ✗SEUs in SRAM-FPGAs affect
  - ●Flip-flops
  - ●User memory
  - ●Configuration memory and thus the logical function of the circuit as well

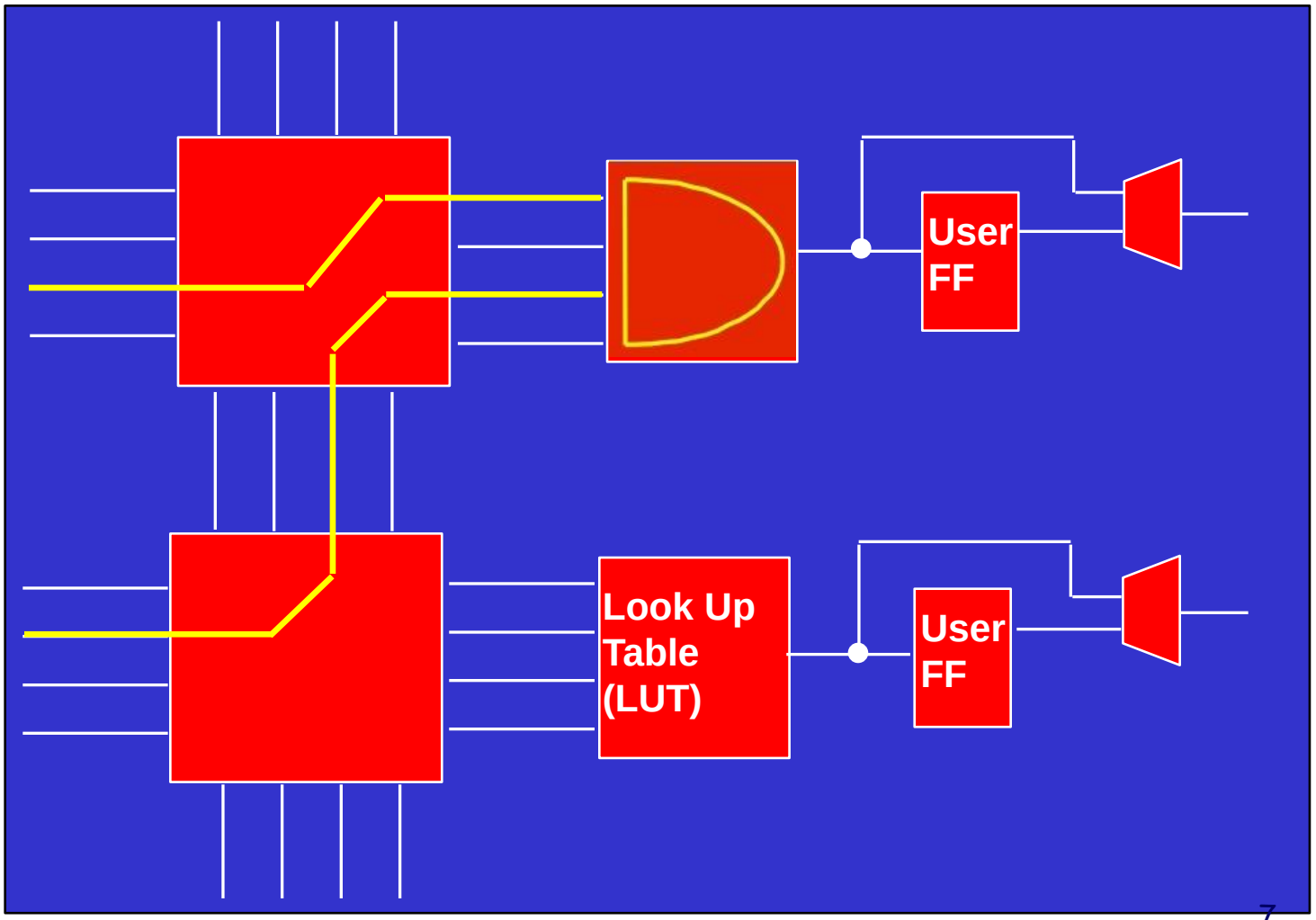
SRAM-FPGAs Architecture



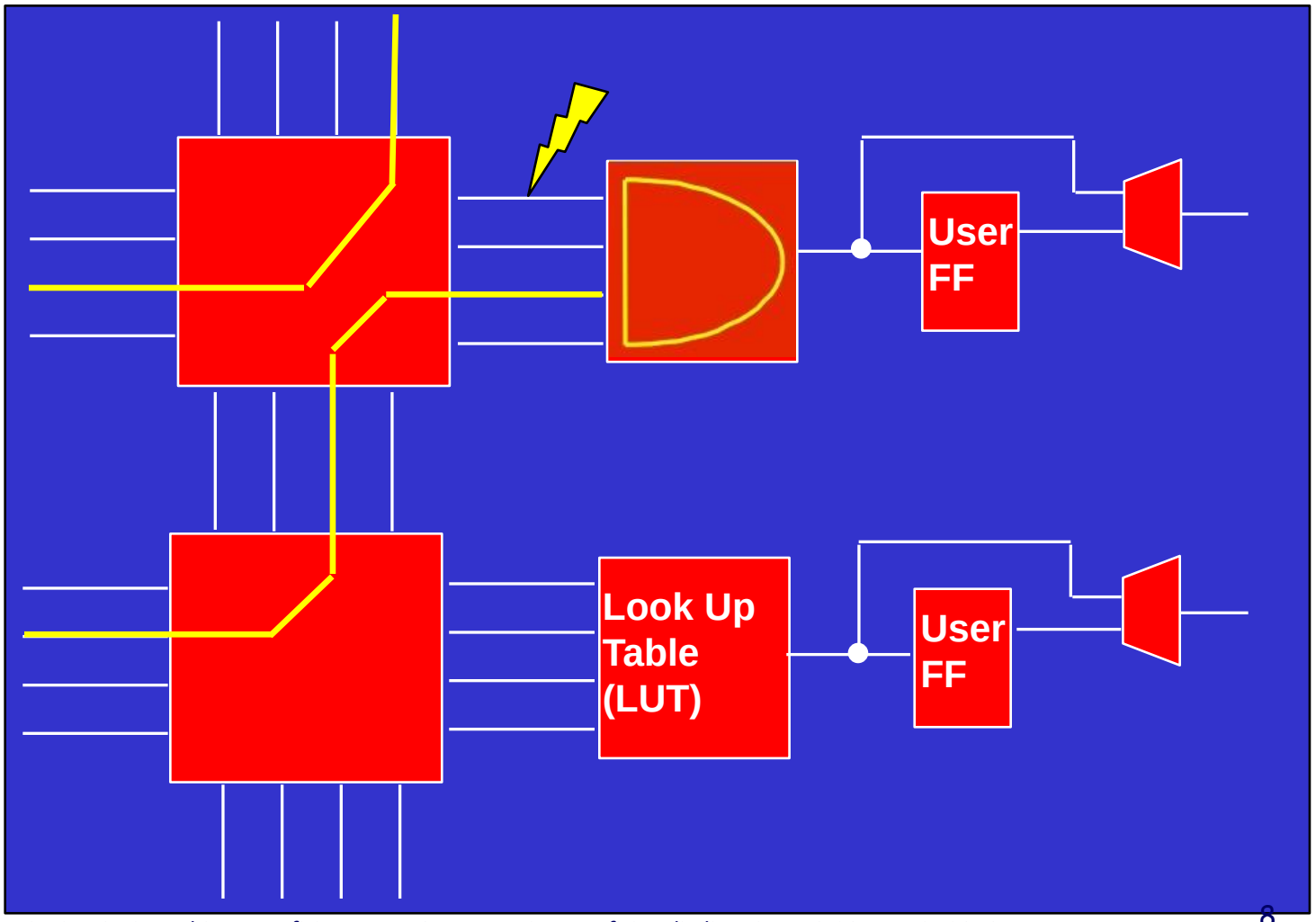
SRAM-FPGAs Configuration Bits



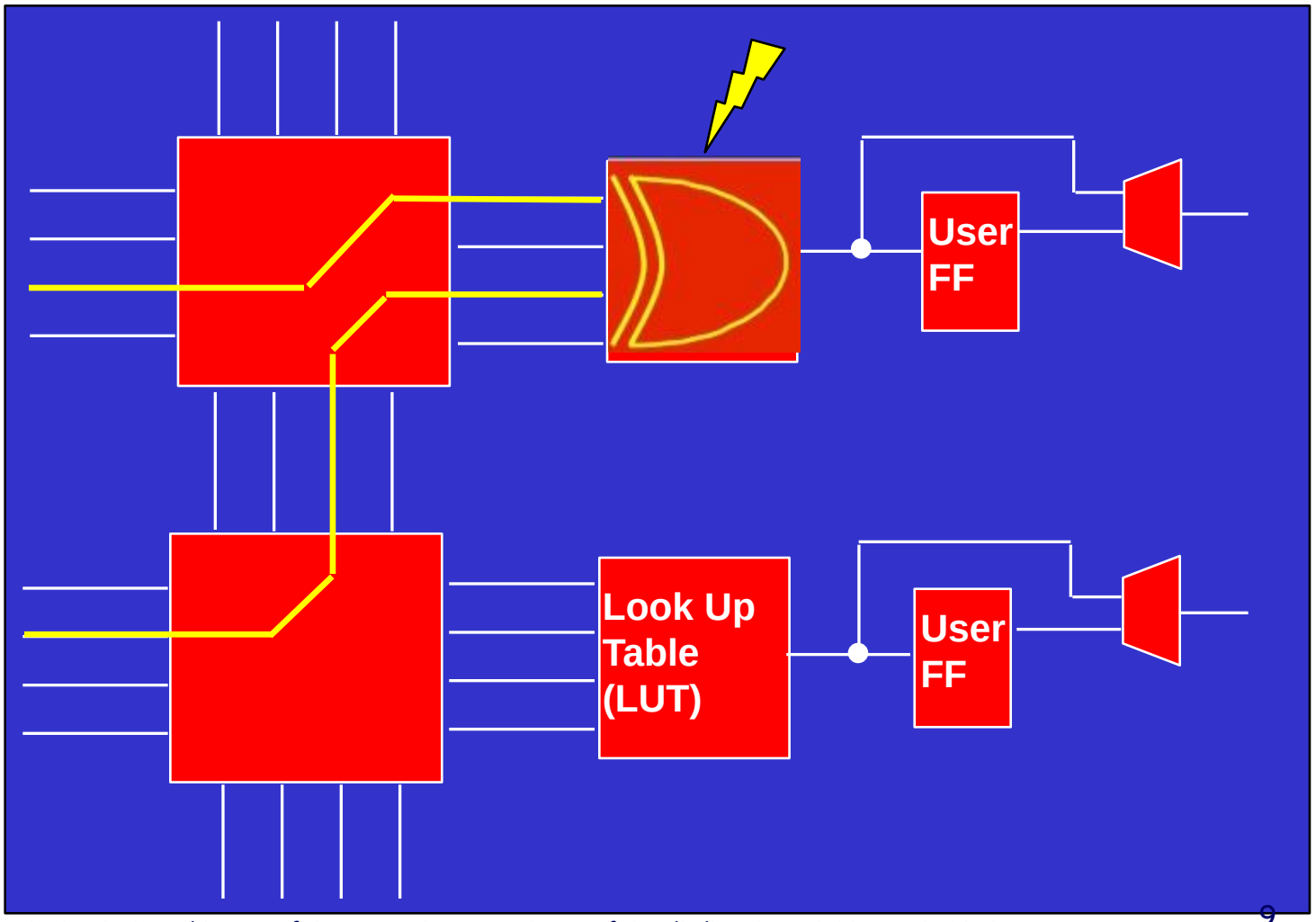
FPGA design



FPGA design – Routing Upset



FPGA design – Logical Upset



A few considerations

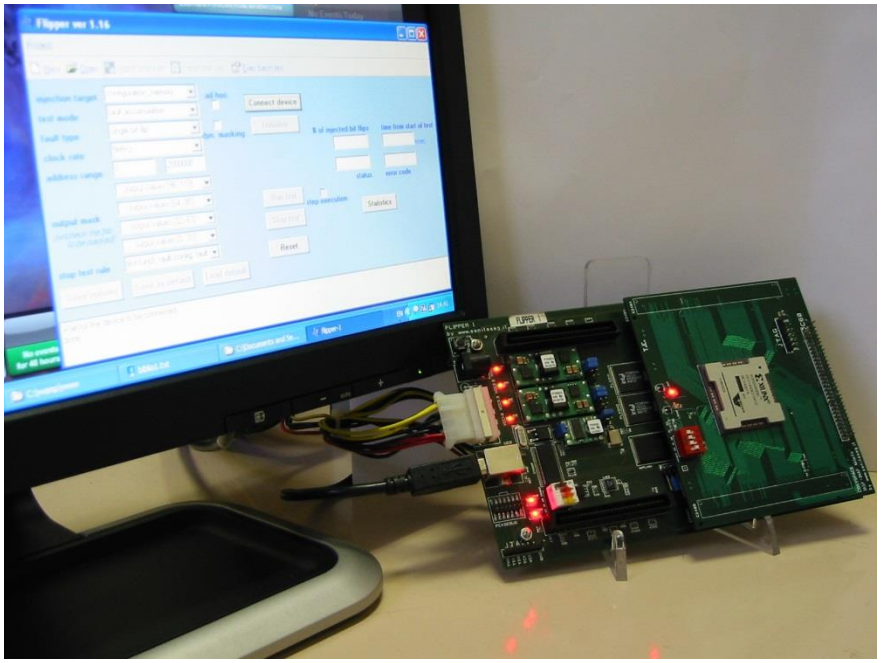
- Not all FPGA configuration upsets affect design behavior
- Only “sensitive” configuration bits will cause a design to fail when upset
- Dependent on design style (mitigation technique, density, etc)
- Tools to evaluate design SEU sensitivity are necessary

FLIPPER

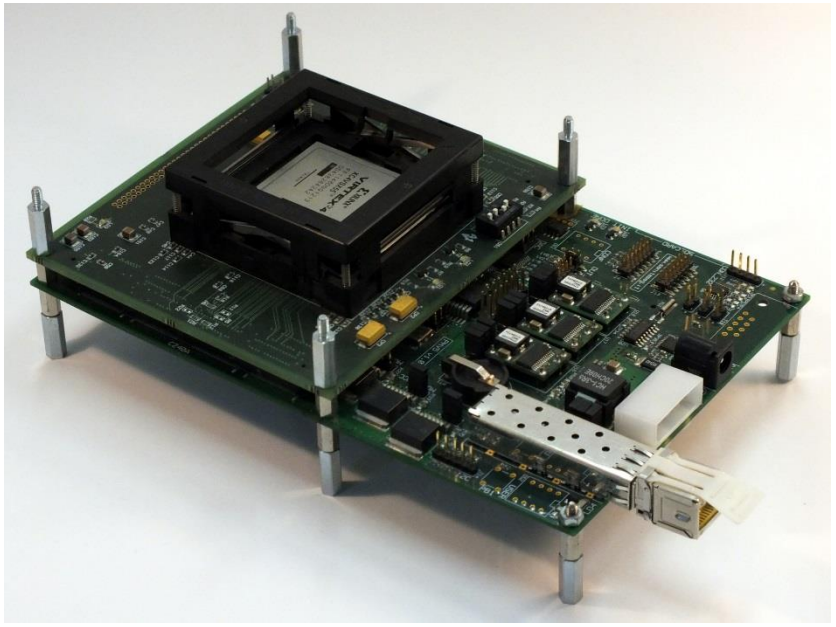
- Fault Injection tool to study SEUs in SRAM-FPGAs
  - ESA/ESTEC contract 18559 (2004-2014)
  - Patent N. 1376923
  - DUT specifically designed for XCV4SX55
  - 1 Gbit/s Ethernet link toward the PC
  - DDR2 SODIMM
- Fault injection by device partial configuration
- The fault model is the bit-flip of configuration memory cells
- Objectives
  - Quantitative characterization of design robustness
  - Comparison of design hardening techniques
  - Tuning of design redundancy and protection

Developed in collaboration with
Sanitas EG

FLIPPER Boards

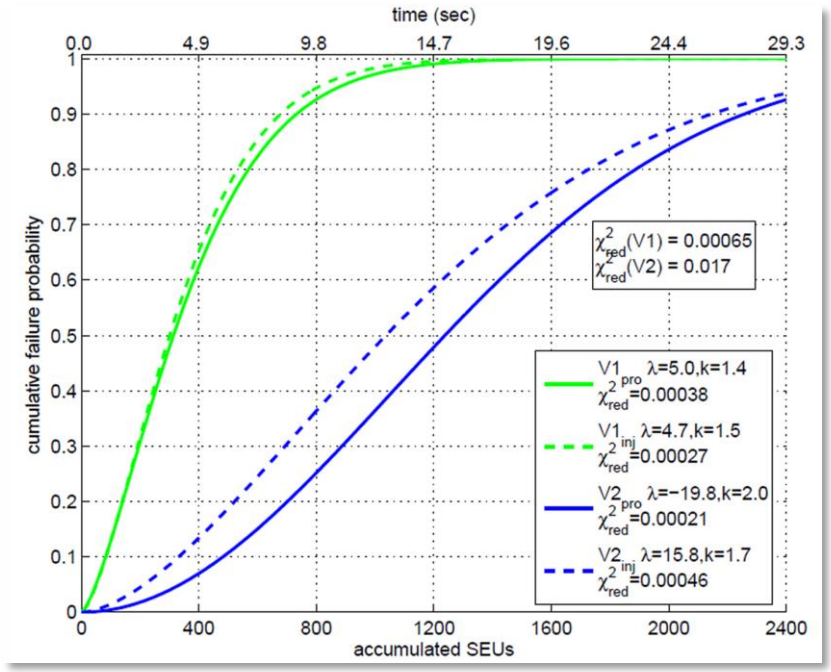


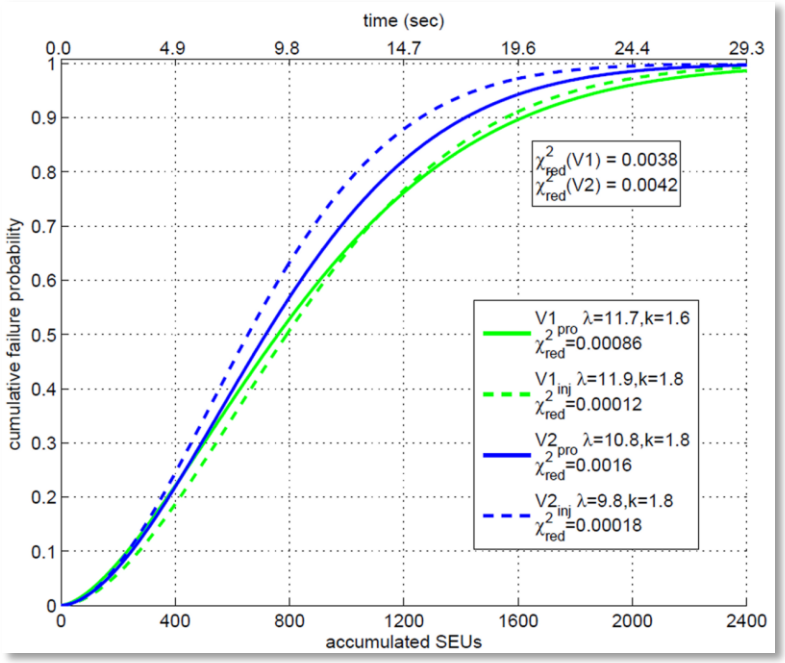
2005



2014

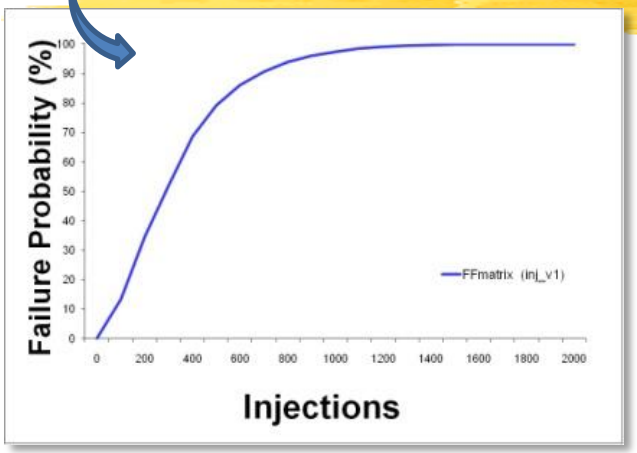
Ffmatrix / FFT



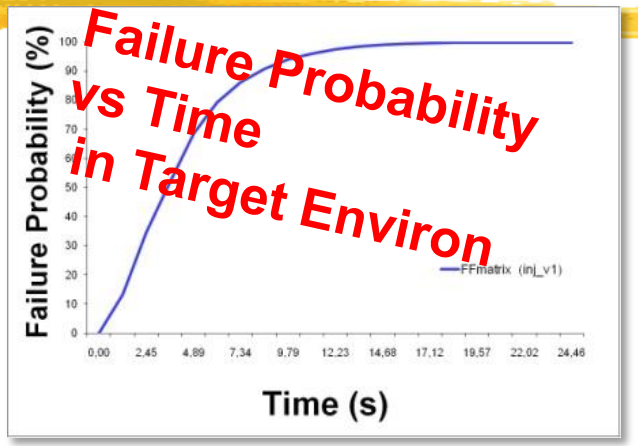


Design Failure Prediction

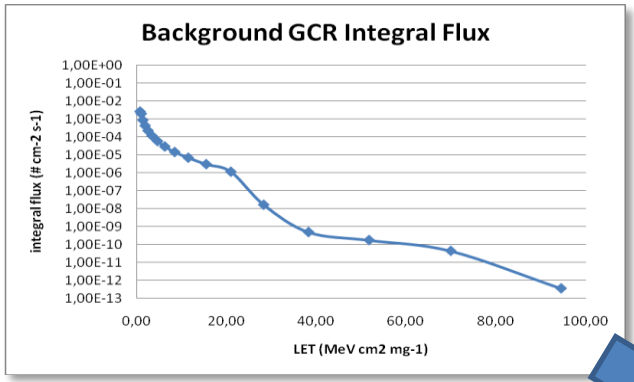
Design Level

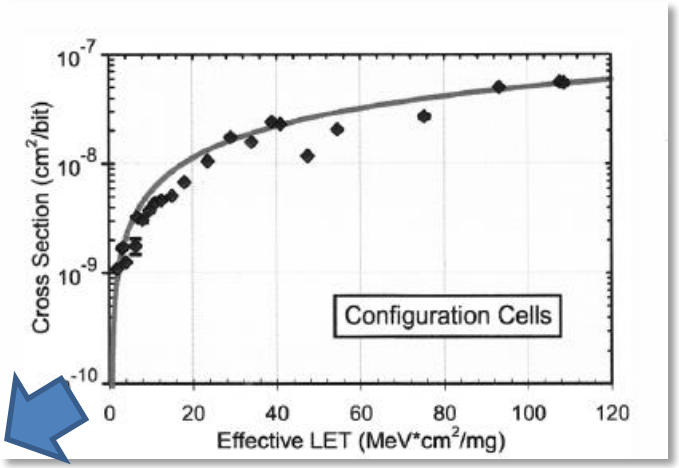


$$t \propto \frac{1}{CBU_{rate}} \cdot n_{inj}$$



Device Level





CBU_{rate}

Hi-Rel CoCs

ESA initiative for using COTS in space

- **Project**: COTS based Computer for On Board systems (CoCs)
- **Objective**: Study and design on-board computing systems based on "Commercial Off-The-Shelf" components
- **Activity phase**:
  1. Design phase: defining the COTS computers as well as the methods for their manufacturing and qualification
  2. Implementation and qualification phase: manufacturing of breadboards that target real missions

- 3 H/W Contracts
  - High Availability Computer - EADS-Astrium Germany
  - **High Reliability Computer - Thales Alenia Space Italia**
  - High Performance Computer - EADS-Astrium France

Hi Rel CoCs Project Team

Prime Contractor: ThalesAlenia Space (A Thales / Finmeccanica Company)

- project management and reporting,
- overall technical coordination
- interface with ESA and the Working Group
- Overall HiRel CoCs detailed specification
- FDIR strategy
- final technology trade-offs and selection
- definition of the CoCs evaluation methods and strategy.

Sub-Contractors:

Dept. of Automation and Computer Engineering of Politecnico di Torino (PoliTo):
- Survey of commercial off the shelf (COTS) processors
- Developing the CoC simulator
- Benchmark SW development

Institute IASF Milano/INAF
- Survey of Reprogrammable Logic Devices
- Hi-Rel CoCs Evaluation Environment & EGSE Definition
- EGSE Development

Department of Electronic Engineering & ULISSE Consortium of the University of Rome "Tor Vergata":
- Survey of candidate Memory Devices
- DDR-II ECC Development

SME company :
- Modeling of Hi-Rel CoCs Building Blocks
- Board and Basic SW Development

PM Module - Major Requisites

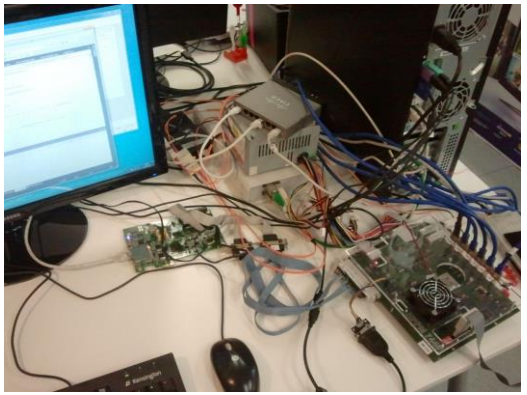
- Outage duration in case of transient failure lower than 10 s
- Mean time between these outages higher than 30 days
- Targeted PM performance: 400 MIPS
- 3 high speed buses (200 Mb/s each), 3 low speed buses (1 Mb/s each), 100 low speed I/O (few kb/s each)
- Lifetime of 15 years
- Reliability better than 0.95 over 15 years

PM Module & EGSE

- CPU based on PPC 7448
- Working memory based on DDR-II
- Use High Speed FPGA (Virtex4) as Bridge
- Virtex4 scrubbing managed by external device
- Combination of SW and HW FDIR strategies
- HW Features specifically supporting SW FDIR
  - Selective Memory Protection
  - Individual Memory power switching to cope with SEFI
  - Smart watch-dog (supervisor) to check program flow
- ESA Standard data Interfaces
  - SpaceWire
  - High Speed Serial links

- PM Board testing/verification
  - To test specific resources of the PM board, such as memory, communications links, and data interfaces
- Benchmarking
  - To test PM board performances when selected benchmarks are applied
- Fault injection
  - To test the response of the PM board in presence of SEU like faults

COTS-Based High-Performance Computing for Space Applications, IEEE Trans. Nucl. Sci., vol. 62 no 6 2015



SBC PowerPC-7448 product definition

- It is the new TAS High Performance Processing Module, based on PowerPC 7448 (2300DMIPS@1GHz core clock), offering performances not available from other European Manufacturers.
- Development has been started in the frame of ESA COTS Based Computer and ARPA ASI Technology program.
- Space Qualified version development is going-on
- Envisageable Applications:
  - Optical Observation payloads
  - Radar Payload
  - Scientific Payloads
  - Planetary exploration Computers
  - Any application requiring high Processing performances

ThalesAlenia Space

iTPM for SKA LFAA

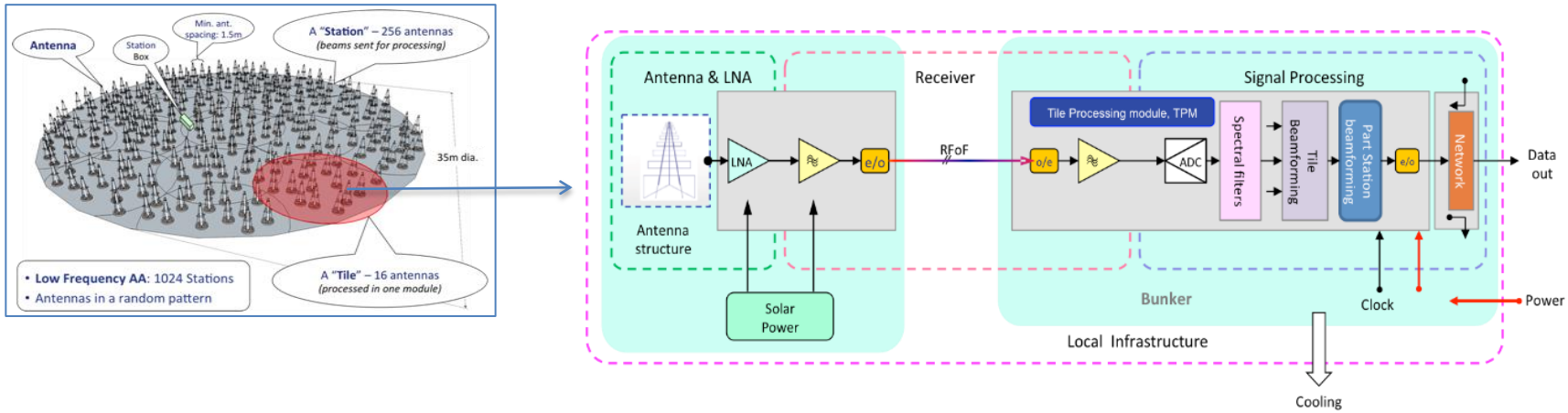
Beginning…

- INAF project approved for funding, May 2013
- **"Digital Platform development for back end design of new generation SKA Aperture Arrays"**
  - 2 year program
  - P.I. Francesco Schillirò (OACT)
  - 5 INAF Institutes involved

- Accepted within LFAA AADC, December 2013 (Signal Processing WP)

AADC Participants and Partners

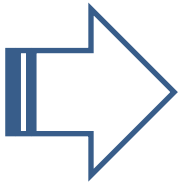
iTPM in LFAA



Tile: 16 Antennas, 2 Pol, 32 Channels

iTPM-ADU first concept, Jan 2014

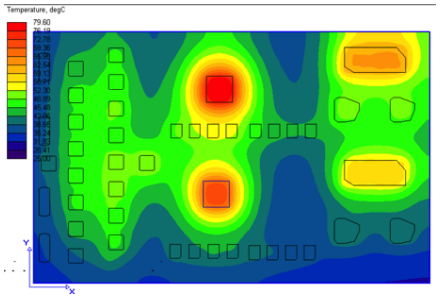
- Main function co-existence:
  - Online digital data processing: 2 large FPGAs
  - Analog to digital low noise conversion
    - 32 analogue inputs
    - Up to 1 Giga sample at 8 bit
  - Board management
- Mechanical specs: max 4U
- Total power < 90 Watt
- Cost, testability & manufacturability

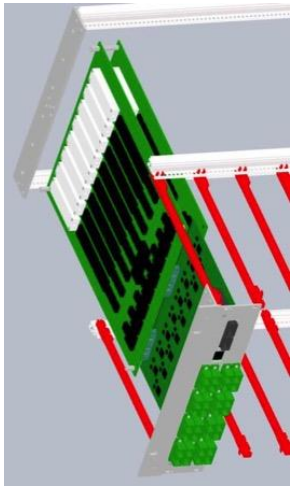


Feasibility study

Feasibility study topics

- Main device: FPGA & AD
- Rack assembly
- Board size & Power dissipation
- Board technology
  - PCB build-up
  - Isolation criteria
  - Sampling clock architecture



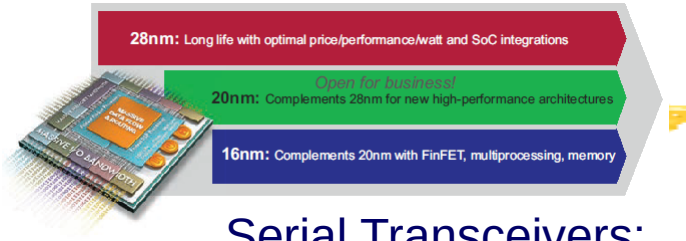


Feasibility output: main devices

- Direct support from market leader suppliers
  - Xilinx: state of the art 20nm Ultrascale FPGA, and early access program
  - Analog Device: last devices close to release
    - JESDB 14 bit 1 GHz dual channel AD
    - JESDB PLL
    - Ultra High PSRR linear regulator for AD
    - SKA DEMO FMC board to performance evaluation

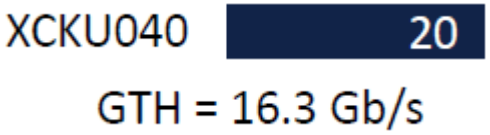
FPGA Xilinx Ultrascale: 20 nm device

Part Number	XCKU040	XCKU060	XCKU075
Logic Cells	424,200	580,440	756,000
CLB Flip-Flops	484,800	663,360	864,000
CLB LUTs	242,400	331,680	432,000
Maximum Distributed RAM (Kb)	7,050	9,180	7,290
Block RAM/FIFO w/ECC (36 Kb each)	600	1,080	1,188
Block RAM/FIFO (18 Kb each)	1,200	2,160	2,376
Total Block RAM (Mb)	21.1	38.0	41.8
DSP Slices	1,920	2,760	2,592



Production 1q 2015

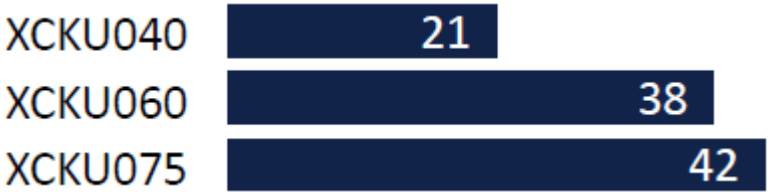
Serial Transceivers:



DSP Slice Count

Speed grade	-1	-2	-3
F_{MAX} [MHz]	594	661	741
Max GMAC/s	6558	7297	8181

Block RAM Capacity (Mb):



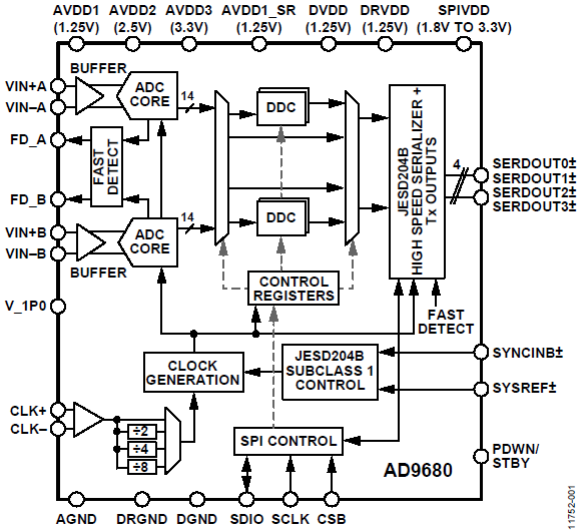
Speed grade	-1	-2	-3
True dual-port Block RAM F_{MAX} [MHz]	525	585	660

AD9680 Datasheet

ANALOG DEVICES

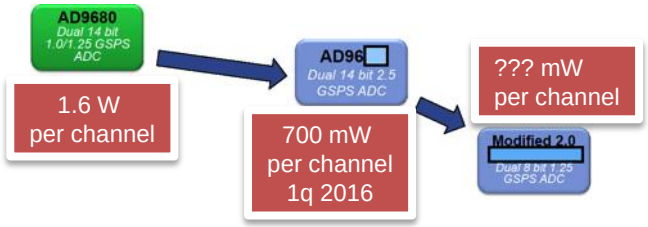
FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.65 W total power per channel at 1 GSPS (default settings)
- SFDR = 85 dBFS at 340 MHz, 80 dBFS at 1 GHz
- SNR = 65.3 dBFS at 340 MHz (A_{IN} = −1.0 dBFS), 61.4 dBFS at 1 GHz
- ENOB = 10.8 bits at 10 MHz
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −154 dBFS/Hz at 1 GSPS
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible input range and termination impedance
  - 1.46 V p-p to 1.94 V p-p (1.70 V p-p nominal)
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 2 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- 2 integrated wideband digital processors per channel
  - 12-bit NCO, up to 4 cascaded half-band filters
- Differential clock input
- Integer clock divide by −1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Small signal dither

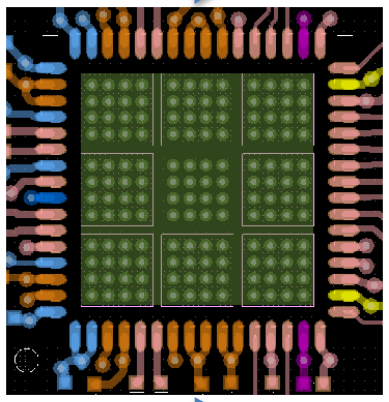


Roadmap to Lower Power

(Power Estimates in SKA Configuration)



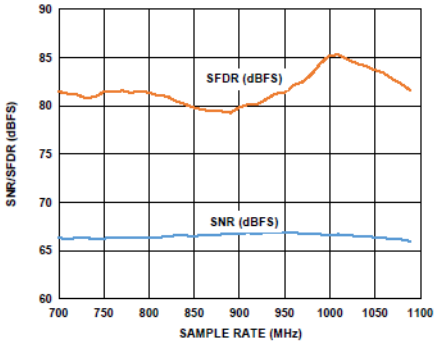
Input 0



Clock

Input 1

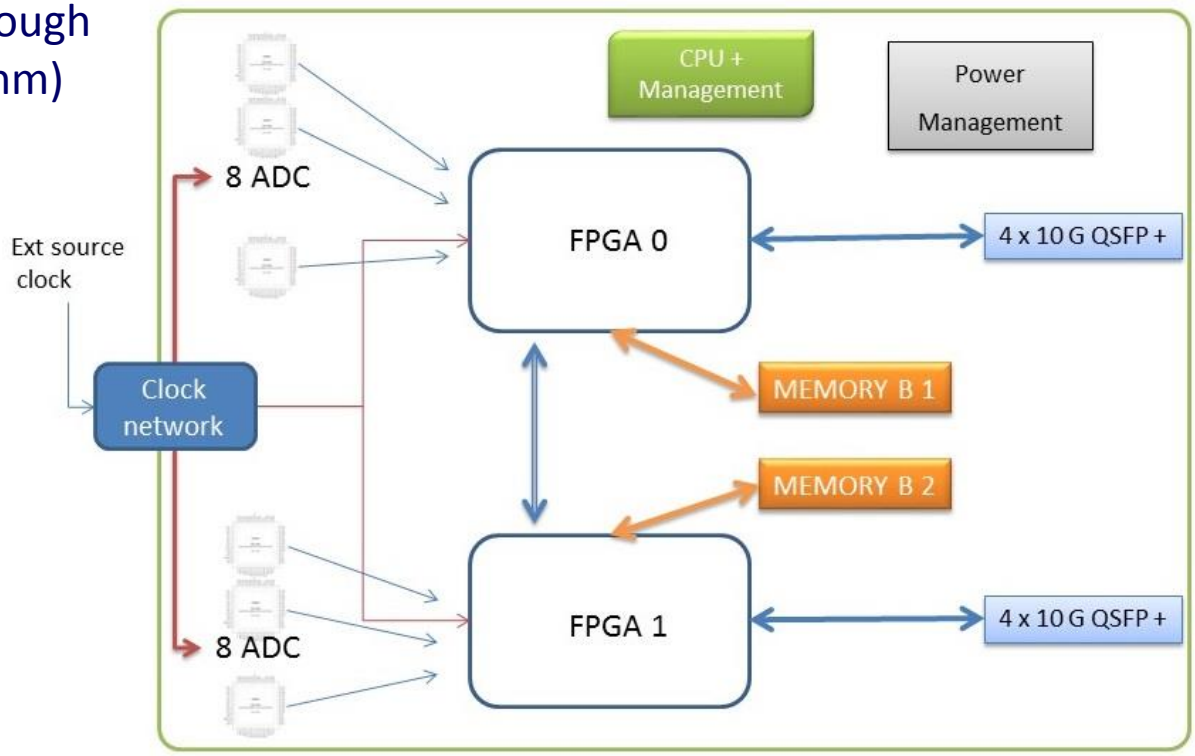
TYPICAL PERFORMANCE CHARACTERISTICS



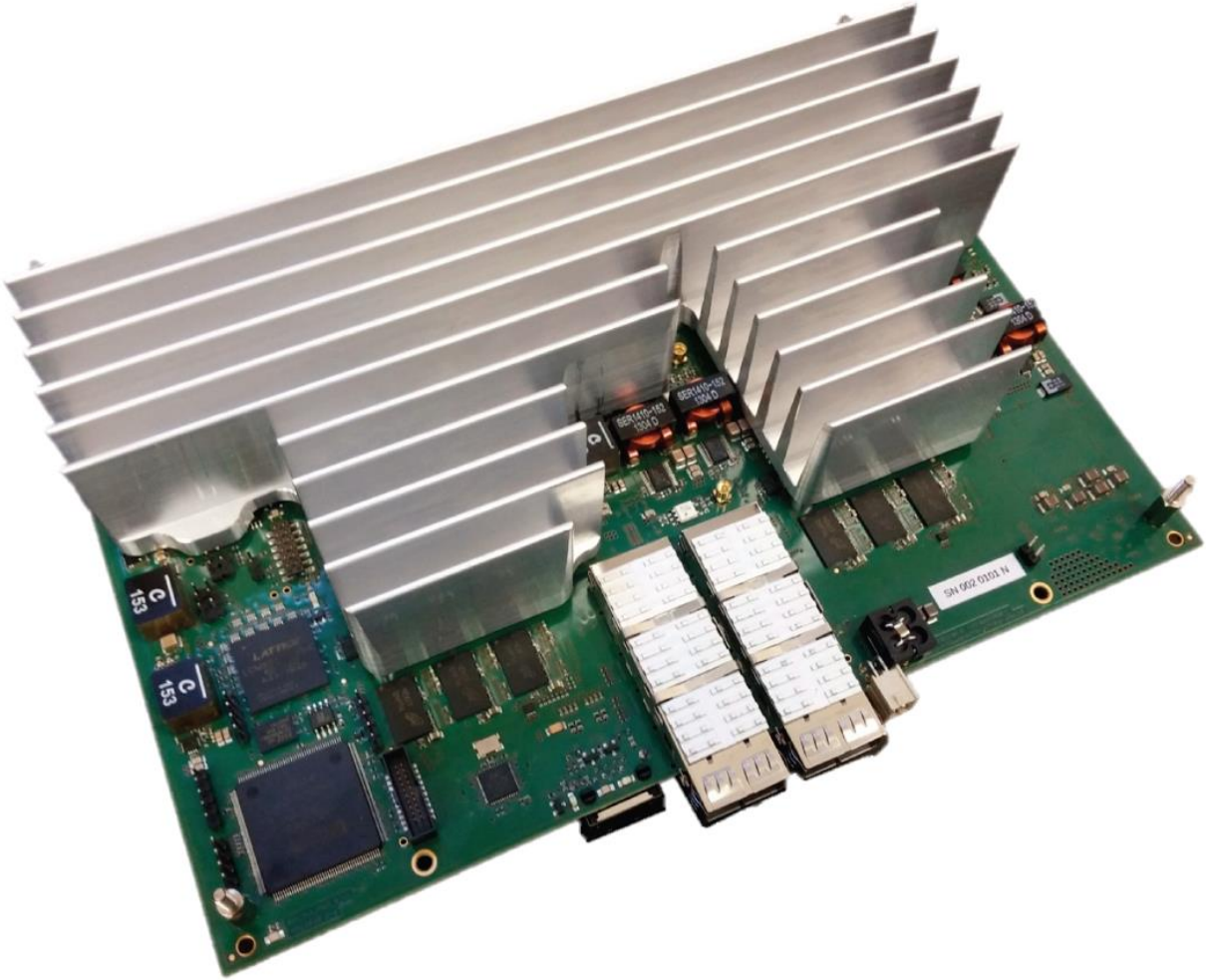
Feasibility output: preliminary board design

- 32 analog inputs with ADC sampling up to 1 Gsample/s
- High speed internal bus for high performance data processing (400 MHz)
- Output communication on high speed digital channels (80 Gbit/s)

- Massive data elaboration through cutting edge FPGA devices (20nm)
- High integration density
- Low power solution



iTPM-ADU



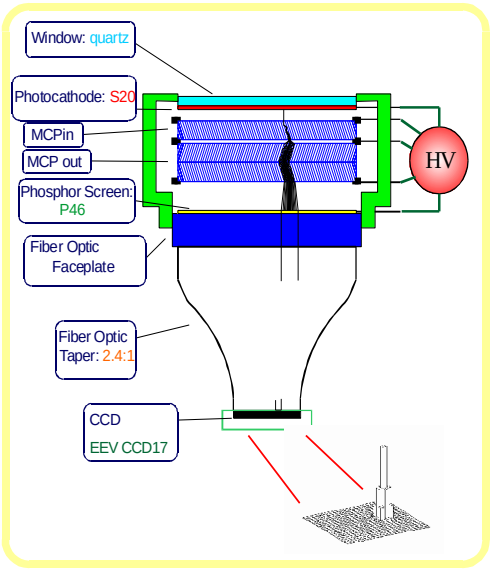
Current & future activities

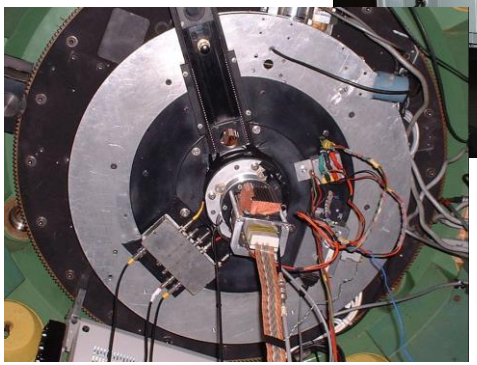
- Public Tender for AAVS1
  - Published April 18, 2016
  - Closure May 18, 2016
- Testing & AAVS1 production support
  - Test Specification
  - Test Firmware
  - Procedures for functional verification of the iTPM ADU board
  - Test JIG development
- iTPM ADU development
  - R 2.0 prototype featuring low power ADCs
  - High density rack capability

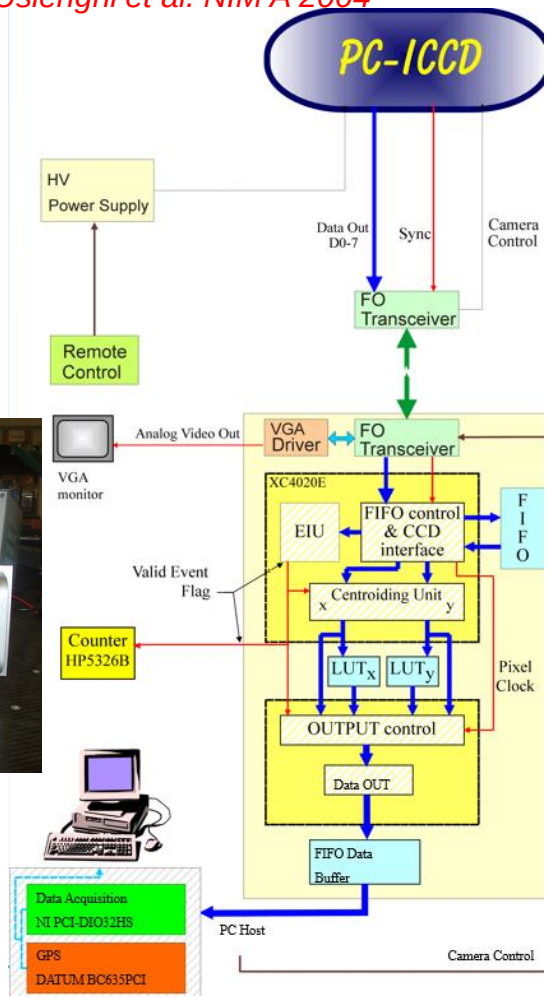
Astronomical detectors R&D involving the use of FPGAs

Wide dynamic range photon counting ICCD for ground-based astronomy, Uslenghi et al. NIM A 2004

- **Photon Counting Intensified CCD** for the optical range, used at the Asiago 182 cm telescope for high time resolution photometry&spectroscopy
  - Xilinx XC4020E used for real time image processing
  - (started 1998, several upgrade, still working)







Astronomical detectors R&D involving the use of FPGAs

MARC: A fast current-readout CMOS front-end for n-substrate, fully-depleted scientific CCDs, Schembari et al.2014 IEEE NSS

- **General purpose detector controller** (based on NI-DAQ system)
  - development of low noise FEEin ASIC for reading CCDs with highly segmented architectures and multiple parallel outputs (PC X-Ray applications) ⇒ System based on National Instruments commercial devices & Labview implementing CCD and ASIC controller, digitalization of the output signal and data acquisition:
    - PXI chassis PXI-1042Q
    - FlexRIO 7952R with digital adapter module NI 6581 (54 single-ended digital I/O channels, up to 100 MHz clock rate) → ASIC sequencer and CCD controller
    - FlexRIO 7952R with ADC adapter module NI 5761 (4 channels sampled at 14 bit, 500 MHz bandwidth and up to 250 MS/s sample rate) → data acquisition

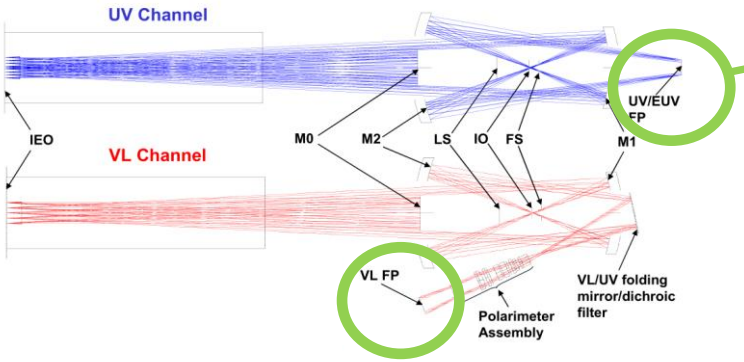
Virtex-5 FPGA

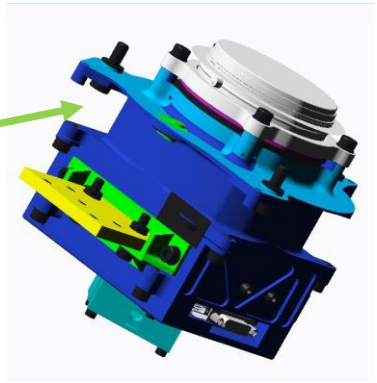
Astronomical detectors R&D involving the use of FPGAs

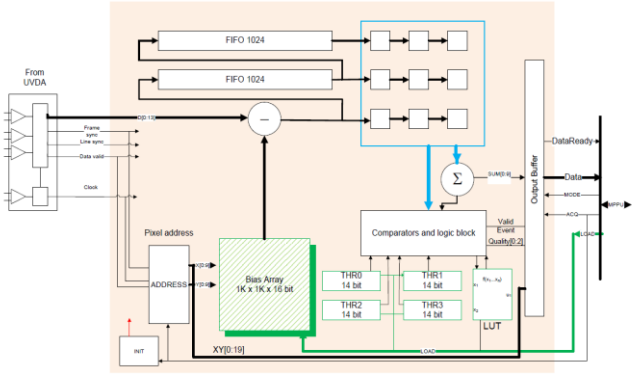
A prototype of the UV detector for METIS on Solar Orbiter, Uslenghi et et al.2012 SPIE 8443

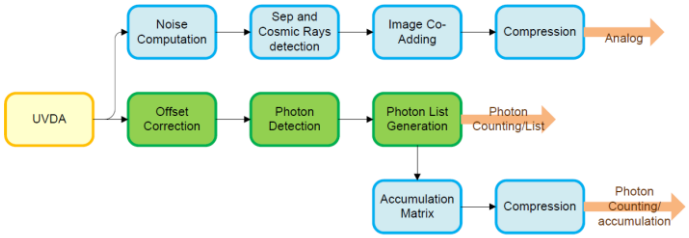
METIS/solar orbiter UVDA:

IAPS 1Kx1K, 30 μm pixel for narrow band images of the Sun corona @ HI Ly-α 121.6 nm (analog & photon counting mode)









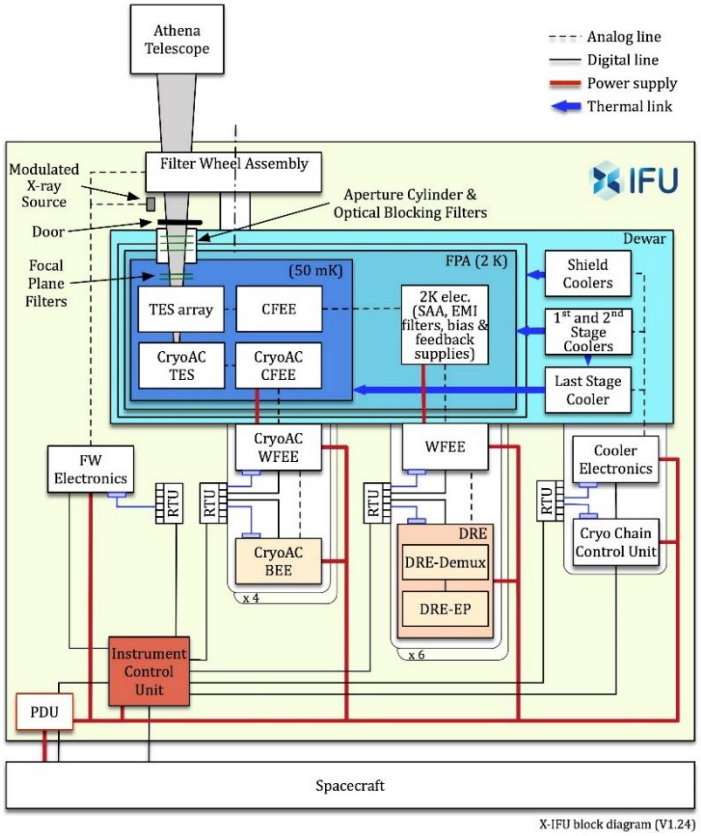
RTAX FPGA

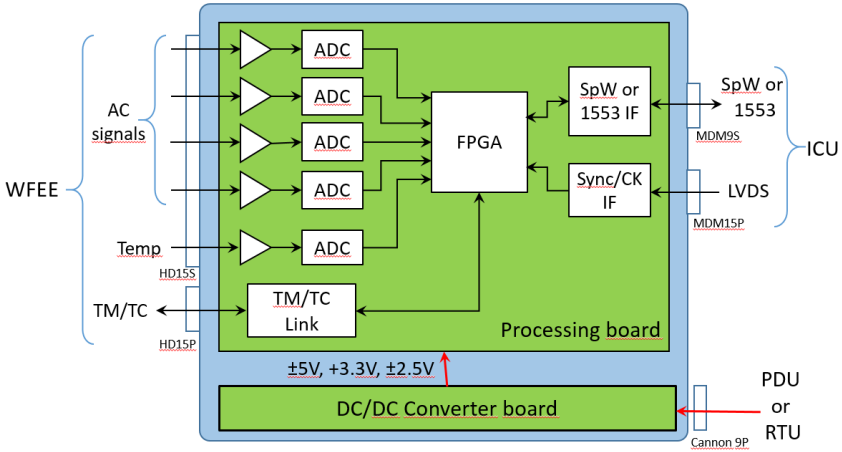
IP core developed with SanitasEG SISTEMI DIGITALI, RICERCA E INNOVAZIONE

- Photon counting algorithms for APS data processing
- UV Flux monitoring flags

Astronomical detectors R&D involving the use of FPGAs (future work)

- Athena XIFU CryoAC BEE





Processing board FPGA-based main tasks:

- Continuous digitization of the four analog signals from CryoAC WFEE;
- Compare the values of the digitized data to a programmable threshold for time tagging and process triggering;
- Processing of the digitized signals to estimate the key parameters of the waveform
- Generation of energy spectra, temporal distribution of the events, ratemeters, etc.
- HK management, TES&SQUID control

THANKS !!!