Centro Nazionale di Ricerca HPC, Big data e Quantum Computing

Spoke Future HPC Kick-off Meeting 29/09/2022

Luca Benini Universita' di Bologna

The better the question. The better the answer.
The better the world works.

Agenda

- 0900-0930 Stato degli accordi, finanziamenti, centri di costo, modalità rendicontazione (30m) **Benini**, **Munna**
- 0930-1015 Organizzare la produzione, la revisione e la sottomissione dei deliverables e milestones (45m) **Benini, Aldinucci, Flagship leaders (Sonza, Silvano, Danelutto, Cilardo, Battiato)**
  - NOTE: Vista l'ampiezza dell'azione è necessario avere una forma di controllo distribuito gerarchico, per esempio organizzato per WP. Dobbiamo definire chi è responsabile di cosa per evitare confusione. Es: Reports scientifici. Timesheet: responsabilità di ogni singolo ateneo, Rapporti tecnici con le aziende della fondazione
- 1015-1030 Discussione sul ruolo degli spoke lab (15min) **Aldinucci, Benini**
  - NOTE: formazione dei giovani, "contamination lab" con aziende, supporto alle attività di tutto lo spoke...
- 1030-1045 break (15 min)
- 1045-1115 Discussione su come organizzare i progetti di "trasferimento tecnologico". (30min) **Aldinucci, Benini**
  - NOTE: Una possibilità è che le aziende elenchino i "need" e i luoghi preferiti di collaborazione, le università le competenze e poi si tenti un matchmaking. Ruolo specifico per gli spoke lab. Possibilità di utilizzare le risorse per affidare parte del lavoro ad aziende piccole esterne al centro in collaborazione con una o più università (outsourcing?), collaborazione a titolo gratuito con aziende interessate (e.g. NVIDIA)
- 1115-1145 Discussione sulle Open call (30min) **Benini, Aldinucci**
  - NOTE: Rivolte ad Aziende fuori dal centro, università fuori dal centro. Proposta: consorzi piccoli (2-4 parterns), con obbligo di coinvolgimento SME/startup che applicano per "challenge" di 6-12 mesi con obiettivi ad alto TRL nell'alveo delle attività definite al punt o precedente (2). Definizione di tempistiche per i bandi e procedure di valutazione e finanziamento.
- 1145-1200. Varie ed eventuali (15min)

COMPOSIZIONE DEL CENTRO

Da finalizzare titoli, leader e partecipanti

In fase di verifica

Partner senza budget

INFRASTRUTTURA
CINECA, INFN, GARR, …

0

3

TITOLI SPOKE	1	2	3	4	5	6	7	8	9	10
	FUTURE HPC	FUND.RESEARCH & SPACE ECONOMY	ASTROPHYSICS & COSMOS OBSERVATIONS	EARTH AND CLIMATE	ENV.&NATURAL DISASTER	MULTISCALE MODELING ENG.APP.	MATERIALS & MOLECULAR SCIENCES	INSILICO MEDICINE & OMICS DATA	DIGITAL SOCIETY & SMART CITIES	QUANTUM COMPUTING
LEADER	UNIBO UNITO	INFN INAF	INAF INFN	CMCC CNR	POLIBA UNIAQ	SAPIENZA UNIPI	CNR SISSA	IIT UNICT	UNINA FBK	POLIMI UNIPD
PARTECIPANTI	POLIMI POLITO UNIPI UNIPD ROMA TOV UNINA UNICT UNICAL INAF CINECA ENEA IIT UNIFE	UNICT UNICAL UNIBA UNIMIB UNINA SAPIENZA UNITS UNIBO POLIBA INAF UNIFI UNIPD UNIFE	SISSA UNITO UNITS SNS-PI ROMA TOV UNICT	ENEA FBK UNITN INGV *OGS*	ENEA UNIBA UNIFI INGV SAPIENZA *OGS* *UNIPR*	UNIBO POLIMI POLITO UNIPV ROMA TOV UNICAL CNR UNIFI *UNIMORE*	UNIMIB UNITS POLITO UNITO UNIPI UNIFI UNITN UNICAL ENEA *UNIMORE* *UNIPR*	UNIBO UNITO UNIPD UNIPV POLIBA UNIBA INFN CNR FBK UNIFE *UNIMORE* *UNIPR*	UNICT UNIMIB UNITN UNIAQ POLIBA CNR	UNIBO UNIMIB UNIPI UNIPV SAPIENZA UNINA POLIBA UNIBA UNICT INFN CNR INAF CINECA IIT
	15	15	8	7	9	11	13	14	8	16

Education and training, Entrepreneurship, Knowledge Transfer, Policy, Outreach

Tutte le altre attività di servizio, incluse: education & training, knowledge transfer, etc. saranno in capo all'Hub

Spoke 1 – Future HPC

Coordinatori Spoke: UniBo, UniTo

Context:

- According to the EU vision, High Performance Computing rests on five pillars: skills, applications, infrastructure, technology, and federation of resources. All the pillars are represented in the Future HPC spoke.
- The main focus is on the technology pillar across all the layers of standard (i.e. non-Quantum) computing s
- i.e. Applications, which are addressed in other spokes of the center.
- In this focused strategy, the FutureHPC spoke is tightly linked with the work-program of the technological

Skills, Applications, Infra, **Technology**, Federation

Align with EU JU: FutureHPC & Digital Sovereignty

- The technological pillar is crucial for EU digital sovereignty and is paramount for engaging industry in achieving (by 2030) European leadership and autonomy in HPC infrastructure, data and services, as well as for fueling innovation across the computing continuum.

Goals:

- To create new laboratories as an integral part of a world-class national federated center of competence for the advanced codesign of high-performance and high-throughput hardware and software systems, with the goal of strengthening Italy's leadership in the EuroHPC Joint Undertaking and in the data infrastructure ecosystem .
- To explore and roadmap key enabling technologies (hardware and software) for the next-generation of high-performance/high-throughput computing systems: the goal is to design and create proofs-of-concept, prototypes and demonstrators raising the readiness level of the most promising technologies and facilitate industrial take-up and development.
- To collaborate with industry for an innovation strategy not limited to supercomputers, but with a strong impact on large volume markets, such as edge servers, IoT gateways, autonomous vehicles, HPC-enabled cloud and data analysis services that critically need reliable, energy-efficient, high performance computing hardware and software. The goal is to widen Italy's footprint in the Key Digital Technologies (KDT) Joint Undertaking , to consolidate Italy's leadership in the EuroHPC Joint Undertaking, and to ultimately strengthen Italy's competitiveness in advanced computing with an open innovation approach.
- To build up a large pool of talent s with strong expertise on state-of-the-art hardware and software technologies and tools for advanced computing. The goal is to contribute to the reduction of the severe skill gap in this area and to increase the number of highly-trained professionals who are essential for Italy's industrial growth and competitiveness in the digital economy.

Research Topics:

Hardware technologies and Systems

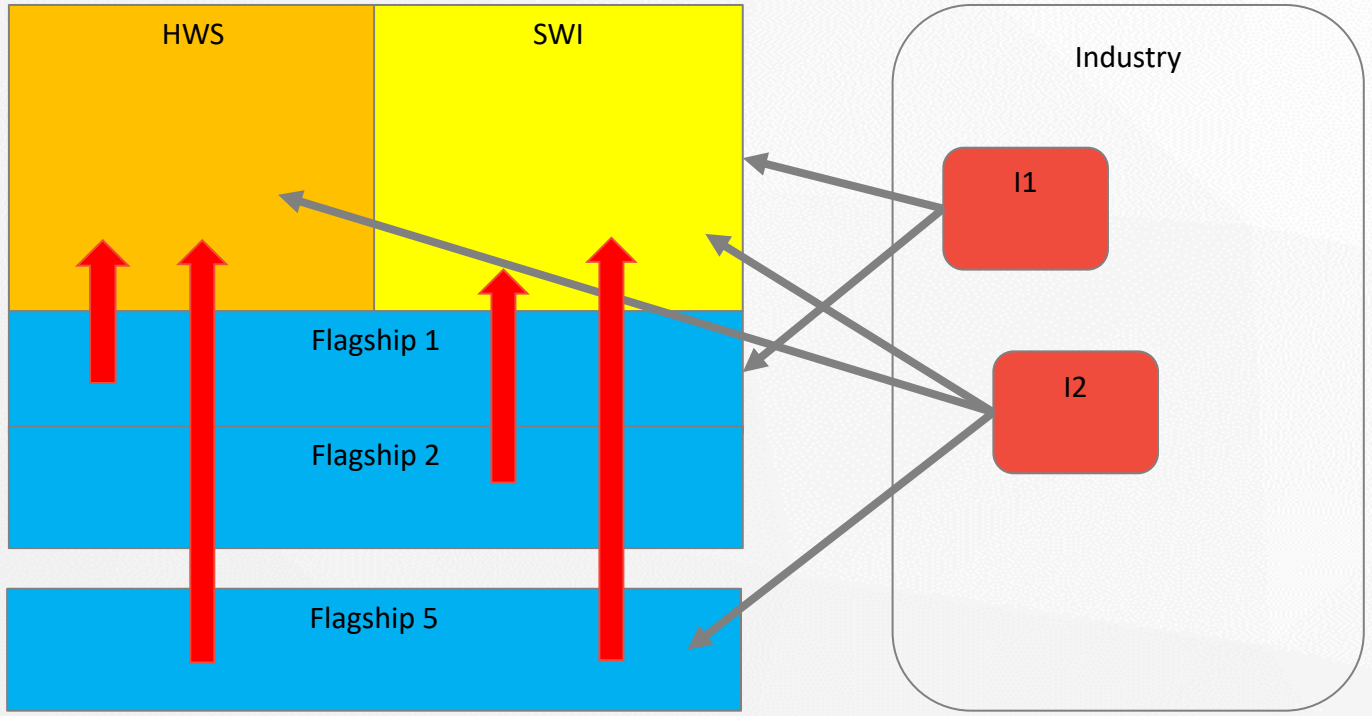
- Computer architecture: Von Neumann, neuromorphic, in-memory, reconfigurable computing. Design of energy-efficient and reliable parallel processors, accelerators, memory and storage hierarchy and interconnects. Open instruction sets (RISC-V), open architectures and open hardware for advanced computing. Integration of classical and disruptive computing technologies: new devices, three-dimensional integration, hybrid quantum/optical/classical computing systems for post-exascale HPC.
- Co-design for added-value HPC and HTC systems: mini-applications design, workload profiling and analysis, hardware optimization and tradeoff analysis, system level performance, power and reliability simulation and design space exploration. Energy-aware hardware-dependent software: energy-efficiency extensions for programming libraries and languages, run-times; energy and power-aware scheduling and resource allocation. Systems for holistic monitoring and management of HPC resources; Data collection systems for power and energy monitoring and accounting.

Software Technologies and Tools

- Programming models for modern HPC applications (shared-memory, message-passing, with-accelerators (e.g. GPU and FPGA); technologies and tools HPC-enabled digital twins; workflow management systems; high-Performance I/O, ad-hoc file systems and high-performance streaming; parallel algorithms and libraries for scientific computing; high-performance compilers and run-time support systems; domain-specific languages and tools, benchmarking and software development methods and optimization for HPC-powered innovative applications; middleware for scalable Big data and AI/DL and their convergence with HPC systems; performance modeling, analysis and simulation for complex parallel systems; heterogeneous computing and resource scheduling; integration of quantum computing kernels into traditional software pipelines; tools and libraries for distributed and Federated Machine Learning.
- Cloud-HPC integration and convergence; data center modelling and management; reliability assessment and predictive maintenance; data-driven autonomics, operator-less configuration and management, anomaly prediction and classification; workload managers (locality-preserving, reservation-oriented, batch+interactive, etc.); multi-tenancy and management of critical data in HPC systems;

Spoke Architecture and Budget

- Two "**Spoke labs**" → research + infrastructure investment and living-labs
  - Bologna (UNIBO/CINECA →TECNOPOLO) HWS: future HPC HW and system prototyping [co-located with HPC facilities]
  - Torino SWI SW integration lab
- 4/5 Multi-partner "**Flagship Initiatives"**
  - Similar to EU projects →objectives, KPIs
- Cascade funding projects



Flagship Initiatives

- **FL1** Non-functional properties - Design exploration: energy, power reliability (performance portability)
- **FL2** Heterogeneous acceleration - architecture, tools, software
- **FL3** Workflow Management System, integration cloud-HPC convergence, High-Performance Storage &IO (filesystems, data movement), Tools for digital twins
- **FL4** Trustworthiness, security, privacy (TEEs vs. homomorphic encryption…) open reference architecture for a Trusted Execution Environment
- **FL5** Codesign - application + SW + HW targeting, benchmarking, patterns, microkernels

Workplans and partnership have been drafted

Spoke Architecture and Budget

- Two "**Spoke labs**" → research + infrastructure investment and living-labs
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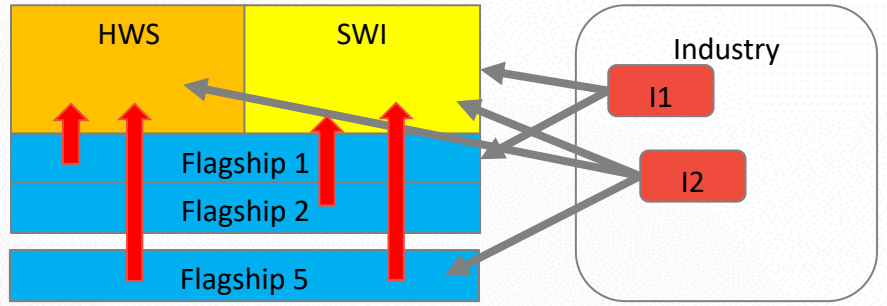
- 4/5 Multi-partner "**Flagship Initiatives**"
  - Similar to EU projects →objectives, KPIs
- Cascade funding projects
- Spoke budget 11.397.000€ + 1.800.000€ + 1.350.000€
  - Spoke leader: personnel + SpokeLab @ Bologna
  - Spoke co-leader: personnel + SpokeLab @ Torino
  - Spoke partners personnel
- Innovation and technology transfer projects 1.800.000€
- PhD funding 2.000.000€
- Cascade funding - calls to be managed by Spoke leader 3.200.000€
- Spoke budget distributed across flagships → allocates effort to flagship initiatives.
- Spoke Labs provide infrastructure (space, equipment) and prototypes, demos, on-site cooperative work…



To be Allocated to activities with companies funding partners of the consortium

To be Allocated to external companies and universities for activities of interest of partner companies and universities

Industry Cooperation (with Founding Members)

1.800.000€

LAB1: Hardware and System Prototyping

LAB2: HPC SW and system software prototyping

Flagship1 - Non-functional properties

Flagship2 - Heterogeneous acceleration

Flagship3 - Workflow management, cloud-HPC convergence

Flagship4 - Trustworthiness, security, privacy

Flagship5 – Codesign, application-SW-HW targeting, benchmarking, patterns, microkernels

1. Evaluate future HPC HW architectures and edge computing
2. Video surveillance system using ML/AI

1. Green Computing
2. Accelerated Computing, OpenSource HW and SW
3. Containers for Cloud continuum, Edge and IoT
4. HPC -Cloud Convergence for Data driven Digital Twin, BigData and AI

1. Scouting future HPC HW architectures and system prototyping
2. Parallel programming models and HPC system software

1. AI andBigData frameworks, integration in HPC ecosystem, federated, distributed learning
2. Mini-applications and benchmarking from multiple domain;

1. Enterprise Multi-tenancy Distributed learning
2. Enterprise AI and BigData frameworks for HPC ecosystem

1. High-performance RISC-V processors for satellite
2. HPC technologies for SAR ground processing of Earth observation data
3. Cyber-security on-board spacecraft, including embedded AI framework and radiation tolerant AI processing in space

1. Cloud-HPC convergence: federated and distributed learning
2. Hybrid MLOps Workflow management & cross-application streaming tools

1. Hybrid HPC Solutions
2. HPC smart sensors and big data
3. Mini applications in naval domain
4. Solutions for onboard power monitoring and control

Cascade funding + Innovation projects

External companies + Research institutions

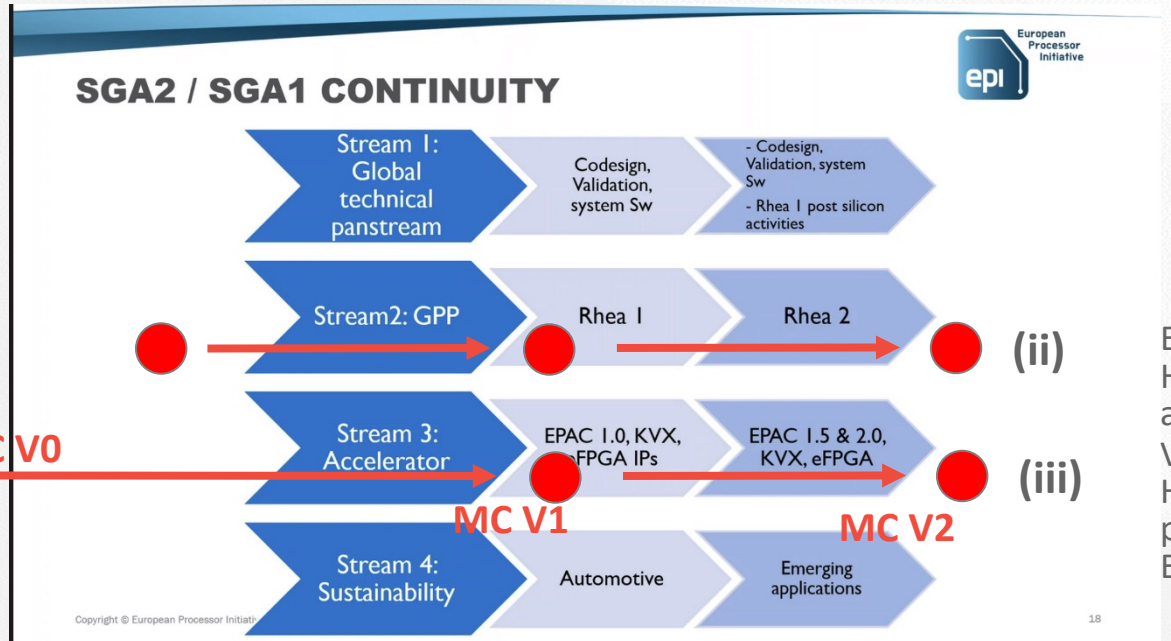
3.200.000€

Status

- Budget cut ~10% after negotiation with MUR
- Creation of the CN legal entity (done)
- Statute (done), IP framework (not done)
- Management board, key figures to be nominated (partly done)
- Timeline is very tight – operation formally started 1/9/2022
- Spoke 1 activities to start at the same time
  - First call for cascade funding by the end of the year (?)
  - First round of innovation projects by the end of the year (?)

HWS: future HPC HW and system prototyping (Managed by UNIBO)

- **Mission:** prototyping HW and system integration (software stack + power management and monitoring)
- **Technical focus**: Open (RISC-V) &Heterogeneous (accelerated) systems
- Colocation in Bologna's technopole - close to the exascale facilities → HW in "relevant environment" (TRL5+)
- Strong links with EU initiatives
  - EuroHPC on-going projects → SGA2, TEP and future calls (RISC-V processors → SGA3-2022)
  - KDT current (21-1-IA focus topic 1) & Future calls and up-coming FPA[1] on open HW (TBD)
- Budget
  - Space Adaptation, Furniture (300K), Workplace: PCs, Printers (150K), Admin/Technical Support + Operation
  - Prototypes: (i) RISC-V host + accelerator(s), (ii) ARM host + RISC-V accelerator, (iii) RISC-V host + accelerators



Example: Monte Cimone HPC system prototypes. V0 available now as a basis. V1, V2 will be built using HPC chips prototypes produced by the EPI EuroHPC projects

(1) Framework Partnership Agreement

SW: future HPC SW and system software (Managed by UNITO)

- **Mission:** designing and implementing programming models and system software
- **Technical focus**: workflows, run-time systems, I/O and data management, HPC-cloud/AI/Big Data convergence
- Co-location in Torino's (TBD) → HW in "relevant environment" (TRL5+)
- Strong links with EU and industrial initiatives
  - EuroHPC on-going projects → ADMIRE, ACROSS, TEXTROSSA, EUPEX, TEP → Future SW EuroHPC call
  - Liaison with relevant private bodies, e.g. Fondazione LINKS, Leonardo, Avio, Intel, Dell, …
- Budget
  - Space Adaptation, Furniture (300K), Workplace: PCs, Printers, Admin/Technical Support, Operation
  - Tier-II system: to extend HPC4AI/C3S systems

- 1) HPC4AI: High-Performance Computing for Artificial Intelligence https://hpc4ai.unito.it
- 2) C3S: Centro di Competenza sul Calcolo Scientifco (C3S) https://c3s.unito.it

- Capacità di calcolo globale

- Isole: 2 isole (produzione e sviluppo) con 2 moduli ognuna (HPC e cloud)
- Nodi: 180 server, di cui: 4 nodi con burst-buffers Intel Optane (2TB), 30 nodi con 1.5TB RAM, 30 nodi con 4 GPU, 4 nodi ARM, 4 nodi con NVidia Bluefield2 400Gb/s, 2 nodi RISC-V.
- Cores e Rpeak: 11000 cores Intel (350 TFlop/s FP64) + 124 GPU NVidia A100/A40/V100/T4 (7.5 PFlops/s FP32, 325 TFlops/s FP64)
- Storage: 4 sistemi di storage indipendenti: Lustre, Ceph, Dell Unity, Dell Avamar per un totale di oltre 4PB

(1) Framework Partnership Agreement

Flagship Project #1: Non-functional properties - Design exploration: energy, power, reliability (Leader: POLITO)

- **Mission:** Evaluating and exploring design solutions in terms of non-functional properties (energy, power, reliability)
- **Main technical activities**:
  - Design techniques for energy- and power-efficient reliable parallel architectures, including CPUs, GPUs, DSPs, FPGAs, neuromorphic devices, memory hierarchy and on-chip interconnects
  - Open source models: RiSC-V processors, GPUs, memory hierarchy and on-chip interconnects
  - Design space exploration techniques and tools
  - Reliability evaluation, HW and SW fault tolerance solutions, Dependability against HW- and SW-related faults
  - HW/SW solutions for power and energy monitoring and management; Thermal/power modeling and control
  - Domain-specific models and languages
  - Parallel programming models and tools for energy efficiency, reliability and performance portability
  - Runtime resource management; Autotuning
  - Environmental costs of HPC systems
- **Strong links with EU and industrial initiatives**
  - EuroHPC SGA1 EPI, EuroHPC EUPEX , Textarossa, SGA2 EPI2, FET-HPC-ANTAREX, FET-HPC-RECIPE, H2020 REPHRASE, H2020 uDEVOPS, H2020 MANGO, H2020 RECIPE, EuroEXA, EUPEX, EPI-SGA1, REGALE, EUROEXA
  - **Liaison with relevant industries and institutions:** STMicroelectronics, Intel, Xilinx, NVIDIA, Thales-Alenia Spazio, Leonardo, E4 Engineering, E4 Analytics, Atos, SECO, ProDesign, Huawei, RFI, MBDA, Hitachi, EnginSoft, Trinandable, Avaneidi
- **Partners and effort (% of partner effort):** Leader: POLITO (30%); UNIBO (30%), POLIMI (30%), UNITO (15%), UNIPI 15%), UNIPD(5%), UNINA (10%), UNICT (5%), INAF (20%), CINECA (40%), ENEA (20%), UNIFE (30%)

Flagship #2: Heterogeneous acceleration - Architecture, tools, software (Leader: POLIMI)

- **Mission:** Design, modeling and simulation of heterogeneous accelerators for HPC-cloud systems and edge servers
- **Main technical activities**:
  - Design of heterogeneous HW accelerators: RISC-V-based, GPU-based, FPGA-based; ASIC-based, soft-cores.
  - Crypto-accelerators; Accelerators for Deep Learning; Tensor cores; Ultra-low-power accelerators; Graph analytics accelerators;
  - Disruptive technologies for accelerators: In-memory Computing, Neuromorphic Computing, Chiplets, 3D integration, Silicon nanophotonics networks; hybrid Quantum/conventional Computing;
  - High-level synthesis of HW accelerators;
  - Modeling and simulation tools for heterogeneous multicore systems;
  - Compilers and runtime systems for heterogeneous accelerated systems;
  - Runtime resource monitoring and management for heterogeneous HPC-Cloud-edge systems;
  - Energy- and QoS-aware scheduling over large heterogeneous HPC-Cloud infrastructures and edge servers;

- **Strong links with EU and industrial initiatives**
  - **EuroHPC on-going projects** → Euro-HPC TEXTROSSA, Euro-HPC EUPEX, Euro-HPC-TEP, Euro-HPC-IA Optima, H2020-EuroEXA → Future EuroHPC calls
  - **Liaison with relevant industries and institutions:** Leonardo, STMicroelctronics, Intel/Altera, Xilinx/AMD, NVIDIA, ENI, E4 Engineering, Thales, EnginSoft, Fondazione LINKS;
- **Partners and effort (% of partner effort):** Leader: POLIMI (30%); UNIBO (30%), UNITO (10%), POLITO (20%), UNIPI 8%%), UNIPD(40%), ROMA-TOV (30%), UNINA (14%), UNICT (10%), UNICAL (10%), INAF (40%), ENEA (50%) IIT (45%), UNIFE (30%)

Flagship Project #3 WMS, HPC-cloud and HPC-AI convergence, Streaming and I/O (Leader UNIPI)

- **Mission:** Defining an integrated software stack to support modern HPC applications, HPC-cloud and HPC-AI/BD convergence and building an "umbrella community" for the joint exploitation of achievements
- **Main technical activities**:
  - Workflow management & cross-application streaming tools;
  - I/O tools (bust-buffers, ad-hoc FS, ETC.) and I/O coordination languages;
  - Compilers & libraries;
  - System software: containers & lightweight virtualization technologies, workload managers;
  - Algorithms for system software: scheduling, mapping, deployment, etc.
  - AI and BigData frameworks and their integration in the HPC ecosystem;
  - Federated and distributed learning;
- **Strong links with EU and industrial initiatives**
  - ERC OPT4SMART; EuroHPC ACROSS, Admire, EUPEX, The EU Pilot; H2020 EU-BRA BigSEA; H2020 DITAS; POR-FESR HPC4AI; H2020 ASTRID; H2020 SSICLOPS; H2020 Hexa-X; EU FP7 PROXIMA; ESA HRAF: EDLS Distributed Simulation Federation and Model-driven Engineering Framework Development, Ministero Difesa: Modelling & Simulation a Service: Architettura e Servizi per Training & Experimentation; PON SCOPE, POR RECAS, H2020 RECIPE; SATURN – Smart mAnufacTURiNg, MISE PON (Fabbrica Intelligente) 2020; H2020 FET-HPC ASPIDE, H2020 EFlows4HPC; SKA; LOWFAR; HBP-SGA3; ICEI
  - **Liaison with relevant industries and institutions:** Leonardo, ENI, E4 Computer Engineering, Atos, Relatech SpA, DtoKLab, NTT Data, STMicroelectronics, A3cube, Hitachi, ENAV, Pitch Technologies, IBM, Oracle, Dell, Intel, Meta, Aruba, Google, SECO
- **Partners and effort (% of partner effort):** UNITO (50%); UNIBO (20%), POLIMI (20%), POLITO (30%), UNIPI (40%), UNIPD(5%), ROMA-TOV (30%), UNINA (15%), UNICT (15%), UNICAL (55%), INAF (20%), CINECA (20%), ENEA (30%), IIT (5%), UNIFE (10%)

Flagship #4: Trustworthy High-Performance Computing (Leader: UNINA)

- **Mission:** Introduce an **open reference architecture** enabling trustworthy, privacy-preserving HPC
- **Main technical activities**:
  - develop hardware-level security primitives for trustworthy computing
  - study crypto-based solutions, e.g. oblivious RAM, homomorphic encryption, etc..
  - introduce a comprehensive RISC-V-based Trusted Execution Environment targeted at HPC
  - define security algorithms and protocols for confidentiality, attestation, etc. based on the RISC-V TEE
  - deliver software support and toolflows for application development
  - set up a provisioning infrastructure, e.g. for attestation services (similar to recent Intel's services)
  - support multi-tenancy in HPC/Cloud environments: integration of TEEs in federated learning and cloud
  - explore application domains: privacy-preserving analytics, more..
- **Links with EU and industrial initiatives**
  - **EuroHPC & on-going projects** → HPC4AI, FP7 mPlane; H2020 EnABLES, H2020 MANGO, SATURN – Smart mAnufacTURiNg, MISE PON (Fabbrica Intelligente) 2020 – Target future EuroHPC calls + Cybersecurity calls
  - **Liaison with relevant industries and institutions:** Thales , SECO, Leonardo, Comau, ENI, Huawei, Ditron, STmicroelectronics, MBDA, Elettronica
- **Partners and effort (% of partner effort):** 5 partners, UNITO (10%), POLITO (20%), UNIPD (5%), UNINA (leader, 45%), UNICT (15%),

Flagship #5: Codesign - application + SW + HW targeting, benchmarking, patterns, microkernels (Leader: UniCT)

- **Mission:** Design, modeling and simulation of heterogeneous accelerators for HPC-cloud systems and edge servers
- **Main technical activities**:
  - Benchmarking of accelerators, software optimization in heterogeneous architectures, microarchitecture efficiency, performance analysis and portability, profiling of HPC codes
  - Mini-applications and benchmarking from multiple domains: AI/ML, Big Data, fluidodynamics, multi-scale simulations, data analysis for astrophysics, N-body dynamics, social media network analysis, graph analytics multi-particle, long-range interacting systems; computational geometry; light-matter interaction, low dimensionality systems, quantum materials, numerical analysis, ecc.). Algorithmic prototyping, and algorithmic co-design: simulation, modeling, optimization;
  - Codesign HW Development and exploitation of next generation of HPC systems: VLSI and FPGA-based architectures; CPUGPU algorithms, VLSI and FPGA-based architectures; data-driven parallelism, data affinity and data locality, streaming computation
- **Strong links with EU and industrial initiatives**
  - **EuroHPC on-going projects** → EuroHPC: ADMIRE, Google Award: BROTLI, EU H2020: RI-SoBigData++, NASDAC, AMBEAtion, ModCOMPSHOCK, EUROEXA, EPI-SGA2, EUPEX - PRIN: aHead, AMANDA - Fluid dynamic, ESA: GNSS Signals - PON:Databanc-CHIS, IBISCO, PIIPRO – PISR:PR SuSy
  - **Liaison with relevant industries and institutions:** Leonardo, STMicroelectronics, Google, Huawei, E4 Analytics, IBM, S.A.T.E., GMV NSL, Elettronica, TIM, Thales Alenia Spaces, EnginSoft, E4 Computer Engineering, Atos, SACMI, UNITEC, Philip Morris.
- **Partners and effort (% of partner effort):** Leader: UNICT(55%); UNIBO (20%), UNITO (10%), POLITO (25%), UNIPI (40%), UNIPD(45%), ROMA-TOV (40%), UNINA (15%), PoliMI (20%), UNICAL (35%), INAF (20%), CINECA (40%), ENEA (0%) IIT (50%), UNIFE (30%)