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ASTRI/CTA data analysis on parallel and low-power platforms

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In addition to performing the entire data reduction and analysis chain of data acquired by the ASTRI Cherenkov telescope(s), one of the main goals of the ASTRI/CTA data reduction pipeline is to fit into a versatile data center, obtaining high-throughput and low-power consumption at low-cost. The performance of the processing algorithms, especially those on the low-level stages of the pipeline, can greatly benefit from an implementation on modern many-core parallel computing hardware, such as GPUs. Furthermore, the inherent energy efficiency of these architectures opens up attractive new scenarios when coupled with low-power ARM processors. In this talk we'll showcase the implementation and the results of the GPU-accelerated code for the ASTRI SST-2M prototype pipeline modules. On datacenter-class hardware, either with x86 or ARM CPUs, the software achieves a net speedup of over 25x compared to the original serial implementation, while on an ARM/GPU SoC development board it surpasses real-time processing requirements consuming around 10W. This would make possible to equip an embedded module on the telescope carrying out preliminary data reduction, greatly decreasing the bandwidth required by an array installation.

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